

# Compal Confidential

## NAWE6 Schematics Document

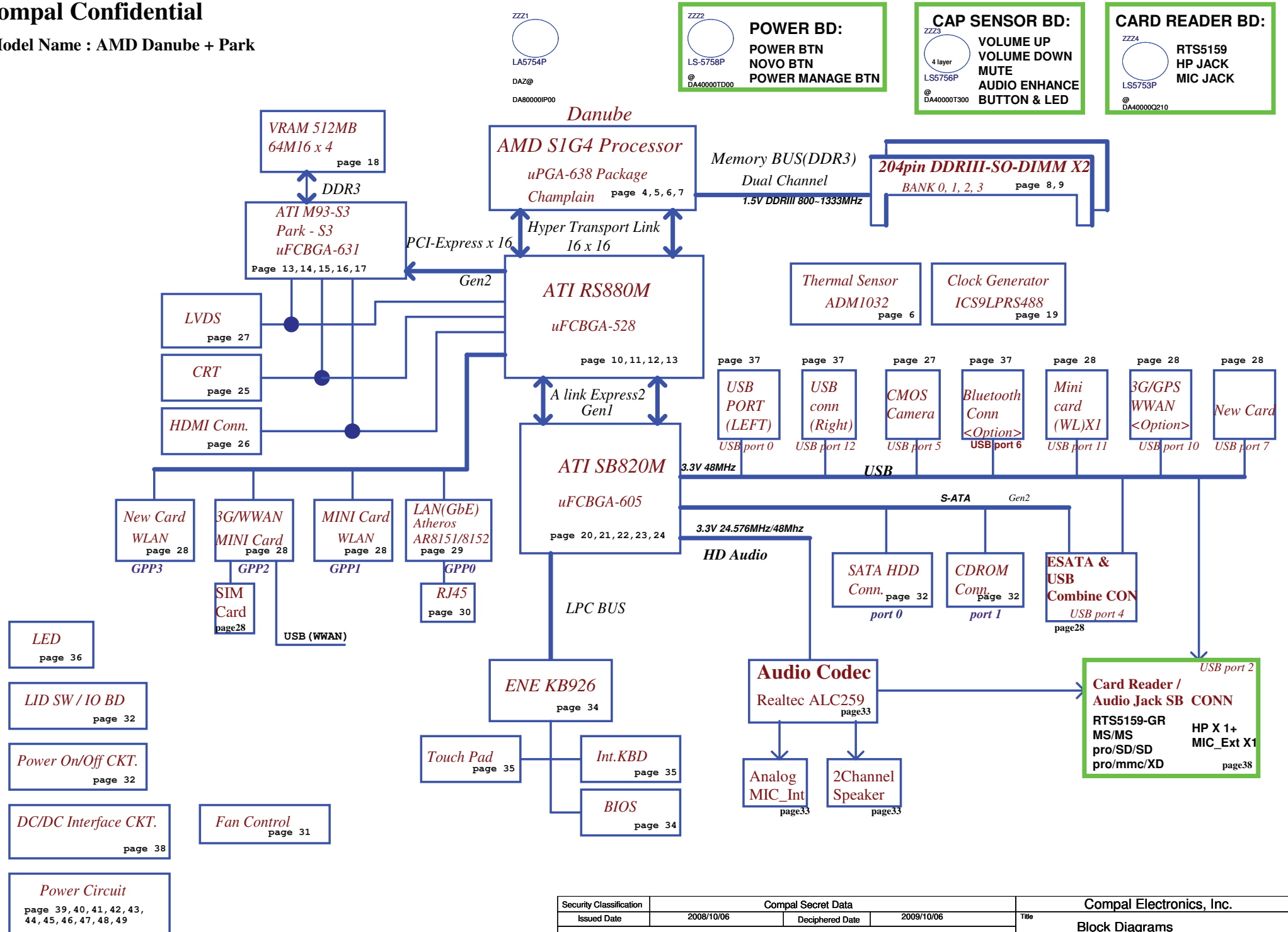
AMD Danube

Champlain Processor with RS880M/SB820/Park VGA

2010-02-24

LA5754 REV: 0.2

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**Model Name : AMD Danube + Park**

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.75VS	+0.75VS LDO power rail for DDR3 VTT	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	EMC1402-1 (CPU)	100_1100b	4CH
			EMC1412-A (GPU)	111_1100b	7CH
			EMC1403-2 (DDR,WWAN)	100_1101b	4DH

EC SM Bus2 address

SB820  
SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2		
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		

SB820  
SM Bus 1 address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Config

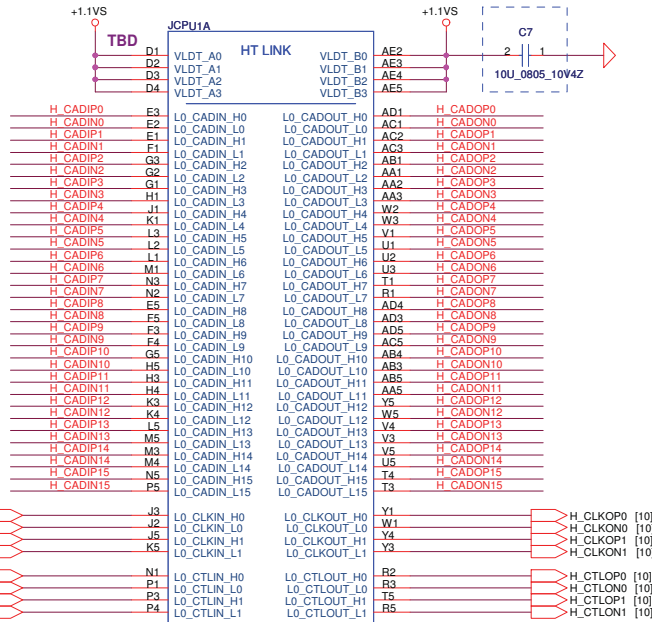
UMA only SKU: UMA@  
DIS ONLY (Park S3): DIS@  
EXT CLK Mode:EXT@  
INT CLK mode:INT@  
LAN GIGA: 8151@  
LAN 100: 8152@  
CMOS@  
BT@  
3G@  
S@  
H@

[10] H\_CADIP[0..15] → H\_CADIP[0..15]

[10] H\_CADIN[0..15] → H\_CADIN[0..15]

[10] H\_CADOP[0..15] → H\_CADOP[0..15] [10]

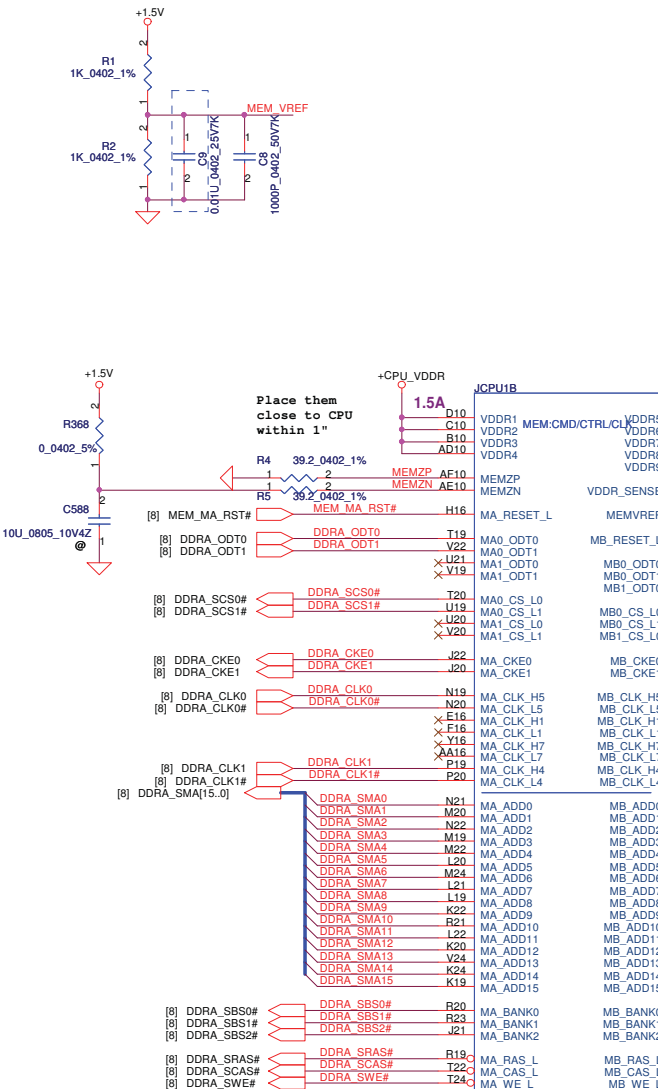
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JCPU1C		MEM.DATA				DDRA_SDQ[63..0] [8]	
DDRB_SDQ0	C11	MB DATA0	MA DATA0	G12	DDRA_SDQ0		
DDRB_SDQ1	A11	MB DATA1	MA DATA1	F12	DDRA_SDQ1		
DDRB_SDQ2	A14	MB DATA2	MA DATA2	H14	DDRA_SDQ2		
DDRB_SDQ3	B14	MB DATA3	MA DATA3	G14	DDRA_SDQ3		
DDRB_SDQ4	G11	MB DATA4	MA DATA4	H11	DDRA_SDQ4		
DDRB_SDQ5	E11	MB DATA5	MA DATA5	H12	DDRA_SDQ5		
DDRB_SDQ6	D12	MB DATA6	MA DATA6	C13	DDRA_SDQ6		
DDRB_SDQ7	A13	MB DATA7	MA DATA7	G13	DDRA_SDQ7		
DDRB_SDQ8	A15	MB DATA8	MA DATA8	H15	DDRA_SDQ8		
DDRB_SDQ9	A16	MB DATA9	MA DATA9	E15	DDRA_SDQ9		
DDRB_SDQ10	A19	MB DATA10	MA DATA10	E17	DDRA_SDQ10		
DDRB_SDQ11	A20	MB DATA11	MA DATA11	H17	DDRA_SDQ11		
DDRB_SDQ12	C14	MB DATA12	MA DATA12	E14	DDRA_SDQ12		
DDRB_SDQ13	D14	MB DATA13	MA DATA13	F14	DDRA_SDQ13		
DDRB_SDQ14	C18	MB DATA14	MA DATA14	C17	DDRA_SDQ14		
DDRB_SDQ15	D18	MB DATA15	MA DATA15	G17	DDRA_SDQ15		
DDRB_SDQ16	D20	MB DATA16	MA DATA16	G18	DDRA_SDQ16		
DDRB_SDQ17	A21	MB DATA17	MA DATA17	C19	DDRA_SDQ17		
DDRB_SDQ18	D24	MB DATA18	MA DATA18	D22	DDRA_SDQ18		
DDRB_SDQ19	C25	MB DATA19	MA DATA19	E20	DDRA_SDQ19		
DDRB_SDQ20	B20	MB DATA20	MA DATA20	E18	DDRA_SDQ20		
DDRB_SDQ21	C20	MB DATA21	MA DATA21	F18	DDRA_SDQ21		
DDRB_SDQ22	B24	MB DATA22	MA DATA22	B22	DDRA_SDQ22		
DDRB_SDQ23	C24	MB DATA23	MA DATA23	C23	DDRA_SDQ23		
DDRB_SDQ24	E23	MB DATA24	MA DATA24	F20	DDRA_SDQ24		
DDRB_SDQ25	E24	MB DATA25	MA DATA25	F22	DDRA_SDQ25		
DDRB_SDQ26	G25	MB DATA26	MA DATA26	H24	DDRA_SDQ26		
DDRB_SDQ27	G26	MB DATA27	MA DATA27	J19	DDRA_SDQ27		
DDRB_SDQ28	C26	MB DATA28	MA DATA28	E21	DDRA_SDQ28		
DDRB_SDQ29	G26	MB DATA29	MA DATA29	E22	DDRA_SDQ29		
DDRB_SDQ30	G23	MB DATA30	MA DATA30	H20	DDRA_SDQ30		
DDRB_SDQ31	G24	MB DATA31	MA DATA31	H22	DDRA_SDQ31		
DDRB_SDQ32	AA24	MB DATA32	MA DATA32	Y24	DDRA_SDQ32		
DDRB_SDQ33	AA23	MB DATA33	MA DATA33	AB24	DDRA_SDQ33		
DDRB_SDQ34	AA24	MB DATA34	MA DATA34	AB22	DDRA_SDQ34		
DDRB_SDQ35	AE24	MB DATA35	MA DATA35	AA21	DDRA_SDQ35		
DDRB_SDQ36	AA26	MB DATA36	MA DATA36	W22	DDRA_SDQ36		
DDRB_SDQ37	AA25	MB DATA37	MA DATA37	W22	DDRA_SDQ37		
DDRB_SDQ38	AD26	MB DATA38	MA DATA38	Y22	DDRA_SDQ38		
DDRB_SDQ39	AE26	MB DATA39	MA DATA39	AA21	DDRA_SDQ39		
DDRB_SDQ40	AC22	MB DATA40	MA DATA40	Y20	DDRA_SDQ40		
DDRB_SDQ41	AD22	MB DATA41	MA DATA41	A20	DDRA_SDQ41		
DDRB_SDQ42	AE20	MB DATA42	MA DATA42	AB18	DDRA_SDQ42		
DDRB_SDQ43	AF20	MB DATA43	MA DATA43	AB18	DDRA_SDQ43		
DDRB_SDQ44	AF24	MB DATA44	MA DATA44	AB21	DDRA_SDQ44		
DDRB_SDQ45	AF23	MB DATA45	MA DATA45	AD21	DDRA_SDQ45		
DDRB_SDQ46	AC20	MB DATA46	MA DATA46	AD19	DDRA_SDQ46		
DDRB_SDQ47	AD20	MB DATA47	MA DATA47	Y18	DDRA_SDQ47		
DDRB_SDQ48	AD18	MB DATA48	MA DATA48	AD17	DDRA_SDQ48		
DDRB_SDQ49	AE18	MB DATA49	MA DATA49	W16	DDRA_SDQ49		
DDRB_SDQ50	AD14	MB DATA50	MA DATA50	W14	DDRA_SDQ50		
DDRB_SDQ51	AD14	MB DATA51	MA DATA51	Y14	DDRA_SDQ51		
DDRB_SDQ52	AF19	MB DATA52	MA DATA52	Y17	DDRA_SDQ52		
DDRB_SDQ53	AC18	MB DATA53	MA DATA53	AB17	DDRA_SDQ53		
DDRB_SDQ54	AF16	MB DATA54	MA DATA54	AB15	DDRA_SDQ54		
DDRB_SDQ55	AF15	MB DATA55	MA DATA55	AB13	DDRA_SDQ55		
DDRB_SDQ56	AF13	MB DATA56	MA DATA56	AB13	DDRA_SDQ56		
DDRB_SDQ57	AC12	MB DATA57	MA DATA57	AD13	DDRA_SDQ57		
DDRB_SDQ58	Y11	MB DATA58	MA DATA58	Y12	DDRA_SDQ58		
DDRB_SDQ59	Y11	MB DATA59	MA DATA59	W11	DDRA_SDQ		

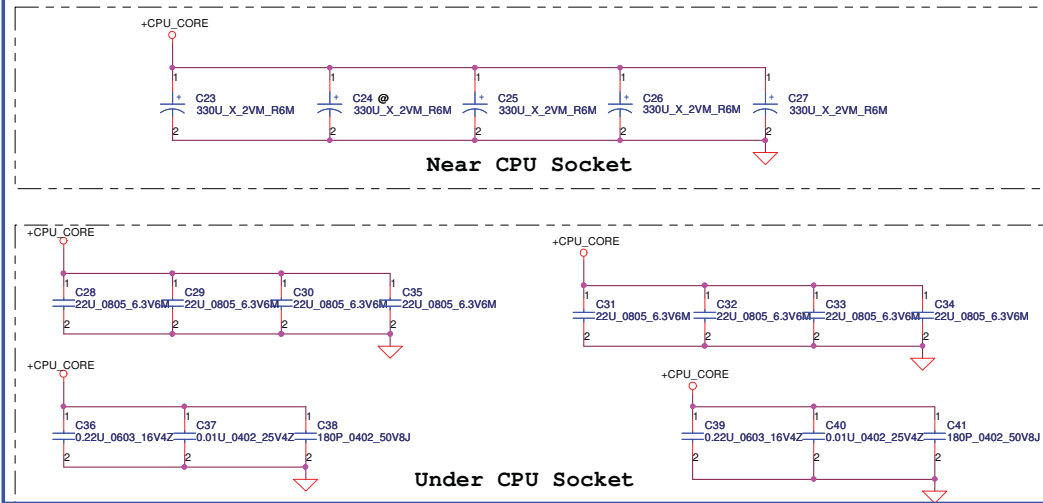


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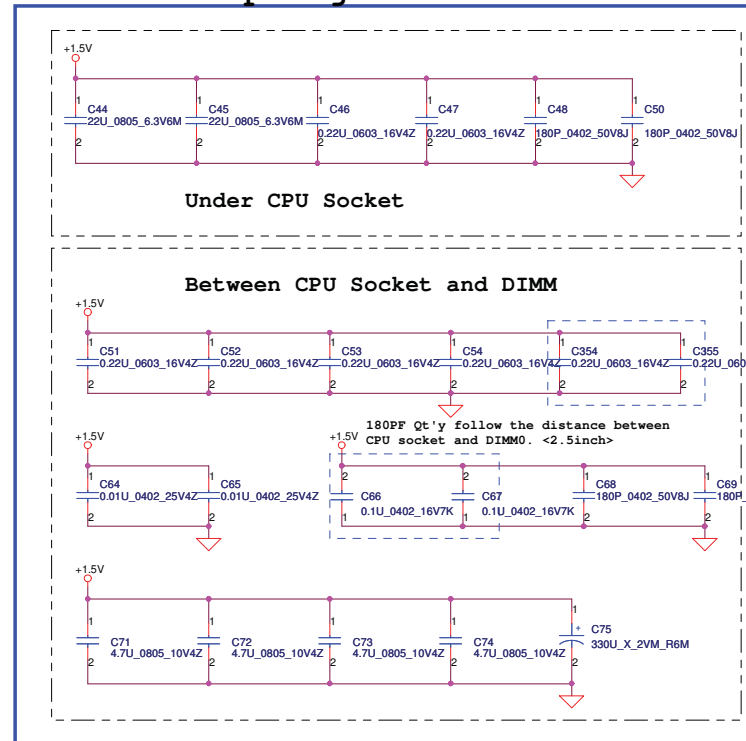
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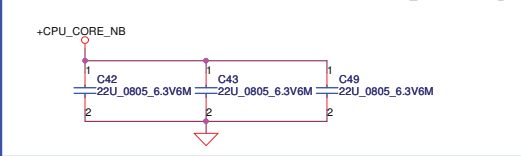
## VDD (+CPU\_CORE) decoupling.



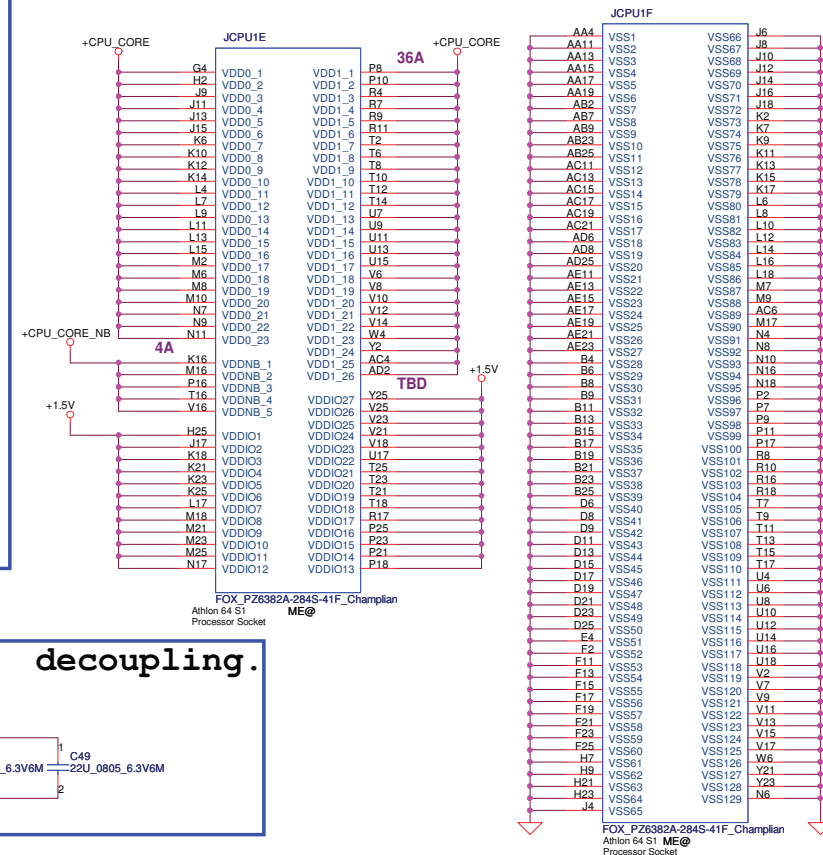
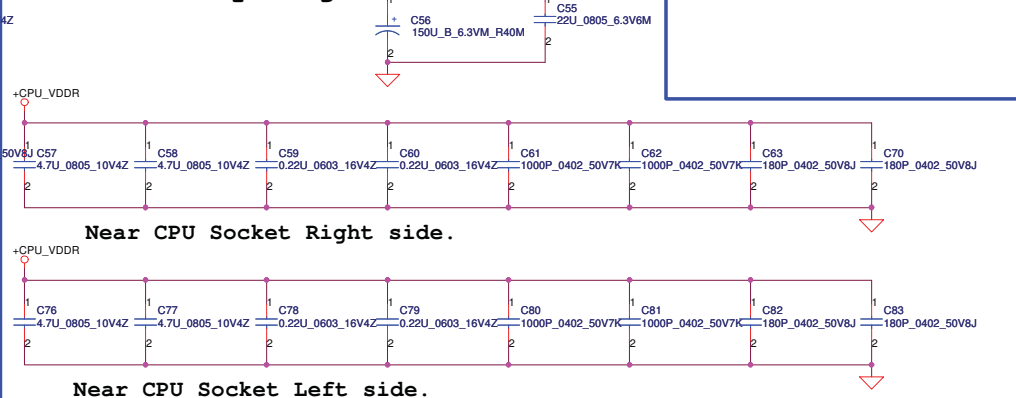
## VDDIO decoupling.



## +CPU\_CORE\_NB decoupling.

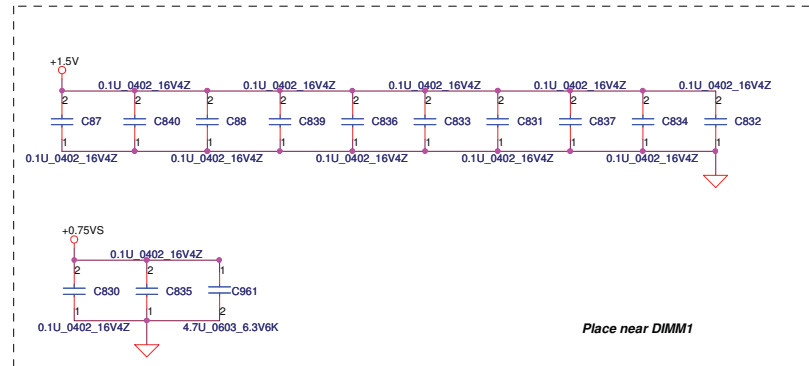
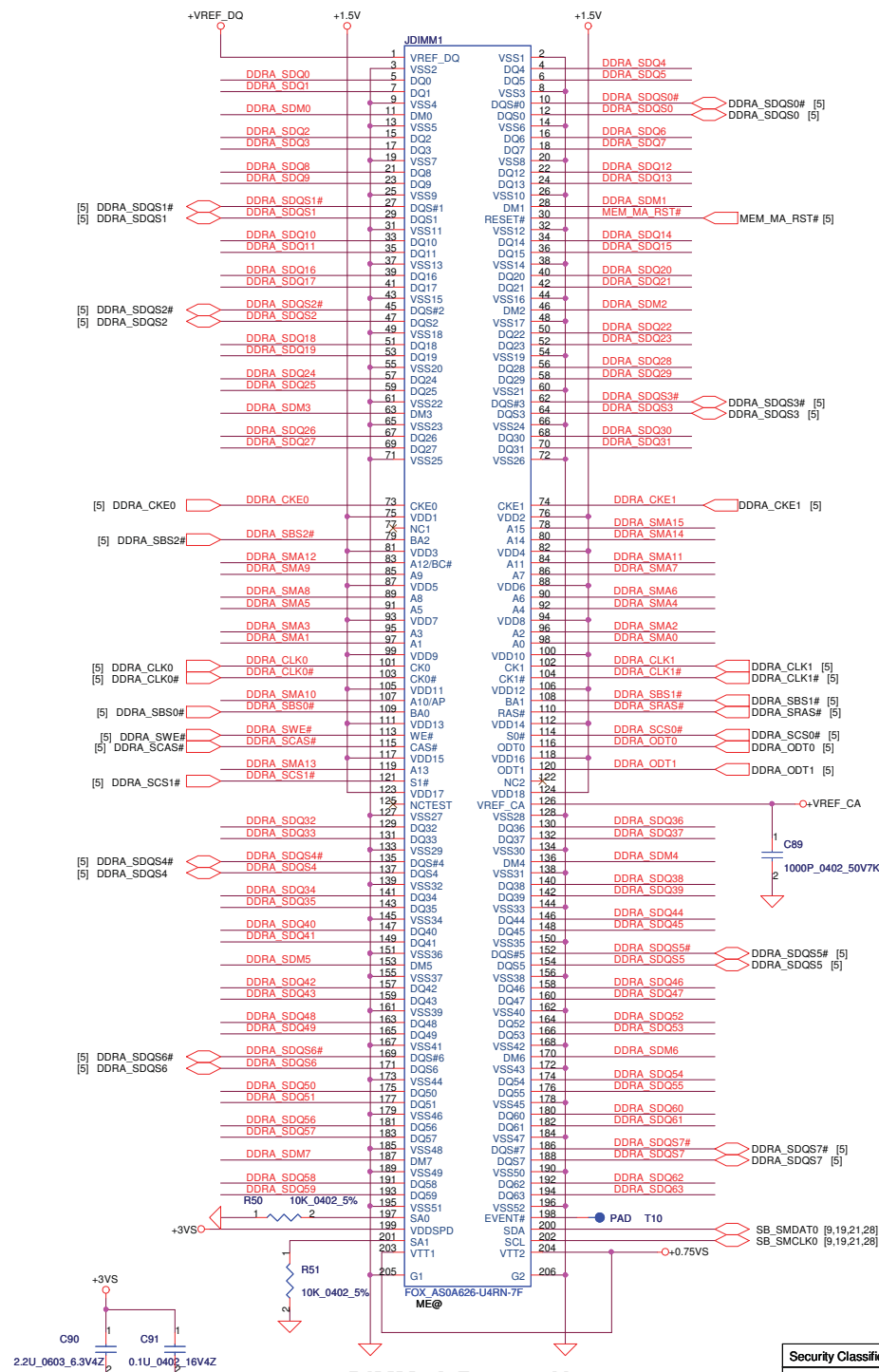


## VDDR decoupling.



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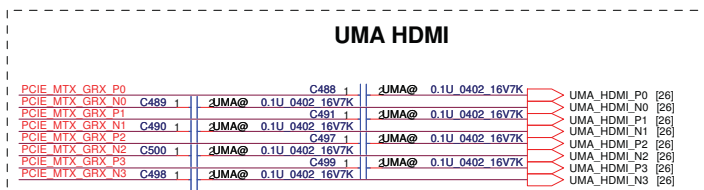
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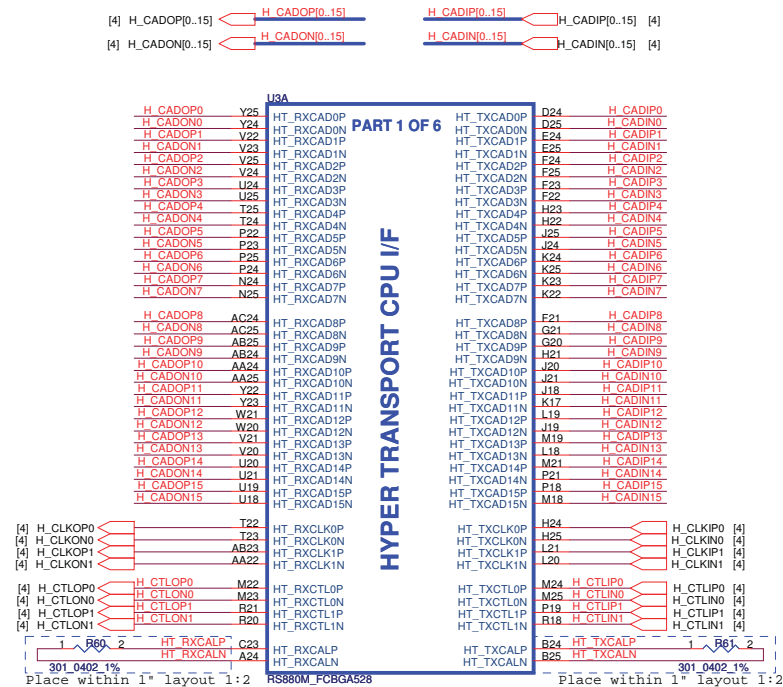
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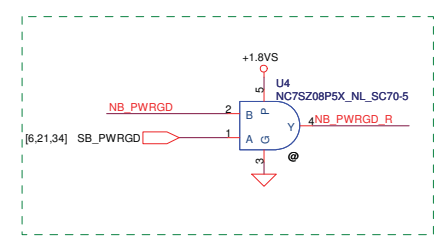
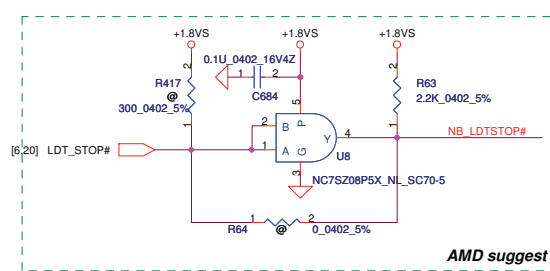
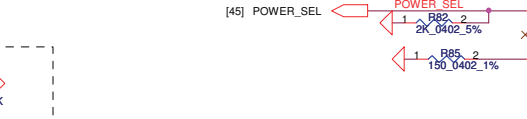
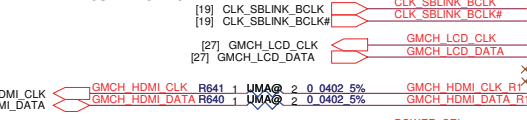
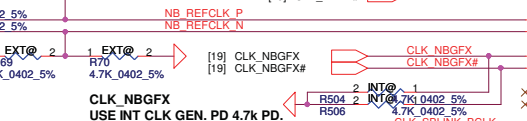
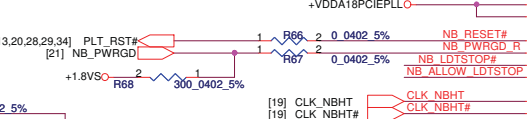
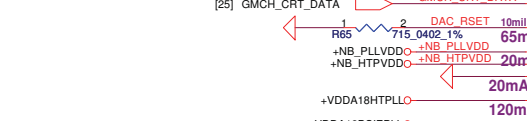
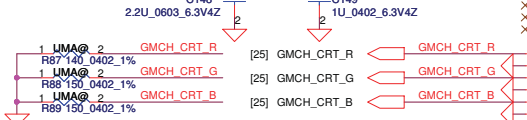
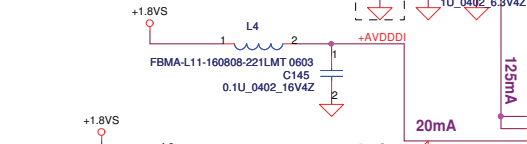
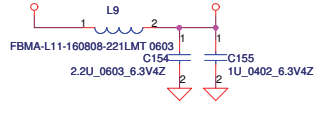
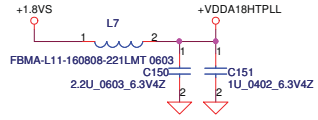
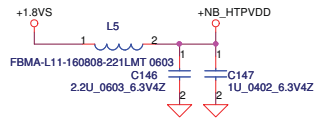
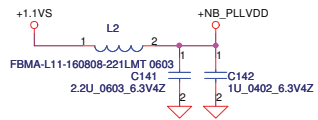


PCIE GTX C MRX P0		D4	GFX_RXP0P	GFX_TX0P0	A5	PCIE_MTX_GRX_P0	C95	1	DIS#	0.1U	0402	16V7K	PCIE_MTX_C_GRX_P0
PCIE GTX C MRX N0	C4	GFX_RX0N	GFX_TX0N	A5	PCIE_MTX_GRX_N0	C96	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N0</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N0</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N0</td>	16V7K	PCIE_MTX_C_GRX_N0	
PCIE GTX C MRX P1	B3	GFX_RX1P	GFX_TX1P	B4	PCIE_MTX_GRX_P1	C97	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P1</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P1</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P1</td>	16V7K	PCIE_MTX_C_GRX_P1	
PCIE GTX C MRX N1	B3	GFX_RX1N	GFX_TX1N	C3	PCIE_MTX_GRX_N2	C100	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N1</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N1</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N1</td>	16V7K	PCIE_MTX_C_GRX_N1	
PCIE GTX C MRX P2	C2	GFX_RX2P	GFX_TX2P	B2	PCIE_MTX_GRX_P2	C101	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P2</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P2</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P2</td>	16V7K	PCIE_MTX_C_GRX_P2	
PCIE GTX C MRX N2	C1	GFX_RX2N	GFX_TX2N	D1	PCIE_MTX_GRX_N3	C102	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N2</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N2</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N2</td>	16V7K	PCIE_MTX_C_GRX_N2	
PCIE GTX C MRX P3	E5	GFX_RX3P	GFX_TX3P	D2	PCIE_MTX_GRX_P3	C103	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P3</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P3</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P3</td>	16V7K	PCIE_MTX_C_GRX_P3	
PCIE GTX C MRX N3	E5	GFX_RX3N	GFX_TX3N	E2	PCIE_MTX_GRX_N4	C104	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N3</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N3</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N3</td>	16V7K	PCIE_MTX_C_GRX_N3	
PCIE GTX C MRX P4	G6	GFX_RX4P	GFX_TX4P	F1	PCIE_MTX_GRX_P4	C105	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P4</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P4</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P4</td>	16V7K	PCIE_MTX_C_GRX_P4	
PCIE GTX C MRX N4	G6	GFX_RX4N	GFX_TX4N	F2	PCIE_MTX_GRX_N5	C106	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N4</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N4</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N4</td>	16V7K	PCIE_MTX_C_GRX_N4	
PCIE GTX C MRX P5	H5	GFX_RX5P	GFX_TX5P	F3	PCIE_MTX_GRX_P5	C107	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P5</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P5</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P5</td>	16V7K	PCIE_MTX_C_GRX_P5	
PCIE GTX C MRX N5	H6	GFX_RX5N	GFX_TX5N	F1	PCIE_MTX_GRX_N6	C108	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N5</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N5</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N5</td>	16V7K	PCIE_MTX_C_GRX_N5	
PCIE GTX C MRX P6	J5	GFX_RX6P	GFX_TX6P	F2	PCIE_MTX_GRX_P6	C109	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P6</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P6</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P6</td>	16V7K	PCIE_MTX_C_GRX_P6	
PCIE GTX C MRX N6	J5	GFX_RX6N	GFX_TX6N	H3	PCIE_MTX_GRX_N7	C110	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N6</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N6</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N6</td>	16V7K	PCIE_MTX_C_GRX_N6	
PCIE GTX C MRX P7	J7	GFX_RX7P	GFX_TX7P	H3	PCIE_MTX_GRX_P7	C111	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P7</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P7</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P7</td>	16V7K	PCIE_MTX_C_GRX_P7	
PCIE GTX C MRX N7	L6	GFX_RX7N	GFX_TX7N	H2	PCIE_MTX_GRX_N8	C112	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N7</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N7</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N7</td>	16V7K	PCIE_MTX_C_GRX_N7	
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PCIE GTX C MRX N8	L6	GFX_RX8N	GFX_TX8N	J2	PCIE_MTX_GRX_N9	C114	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N8</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N8</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_N8</td>	16V7K	PCIE_MTX_C_GRX_N8	
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PCIE GTX C MRX P13	R6	GFX_RX13P	GFX_TX13P	N2	PCIE_MTX_GRX_P13	C123	1	DIS# <td>0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P13</td> </td></td>	0.1U <td>0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P13</td> </td>	0402 <td>16V7K</td> <td>PCIE_MTX_C_GRX_P13</td>	16V7K	PCIE_MTX_C_GRX_P13	
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RS880 A11(SA000032710)

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# PART 3 OF 6

## CRT/TVOUT

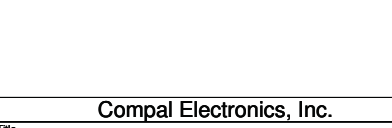
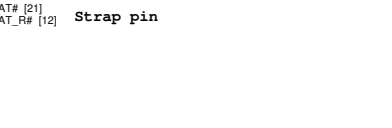
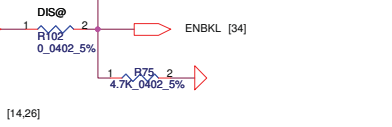
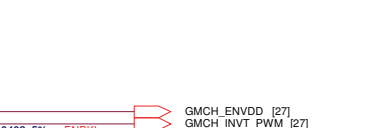
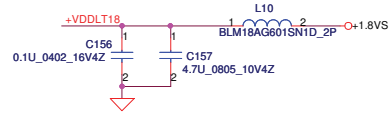
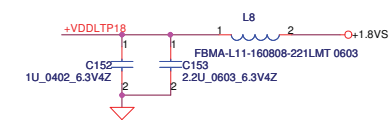
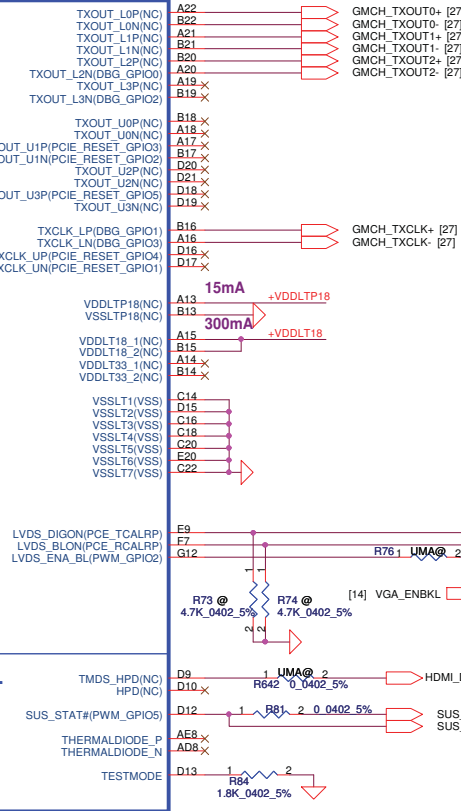
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## PM

## PUL PWR

## CLOCKS

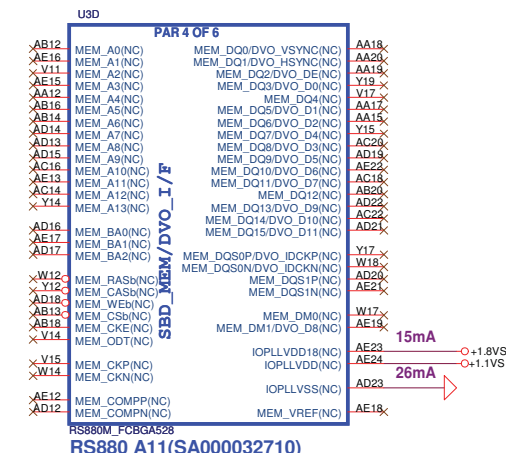
## MIS.



RS880M\_FCBGA528

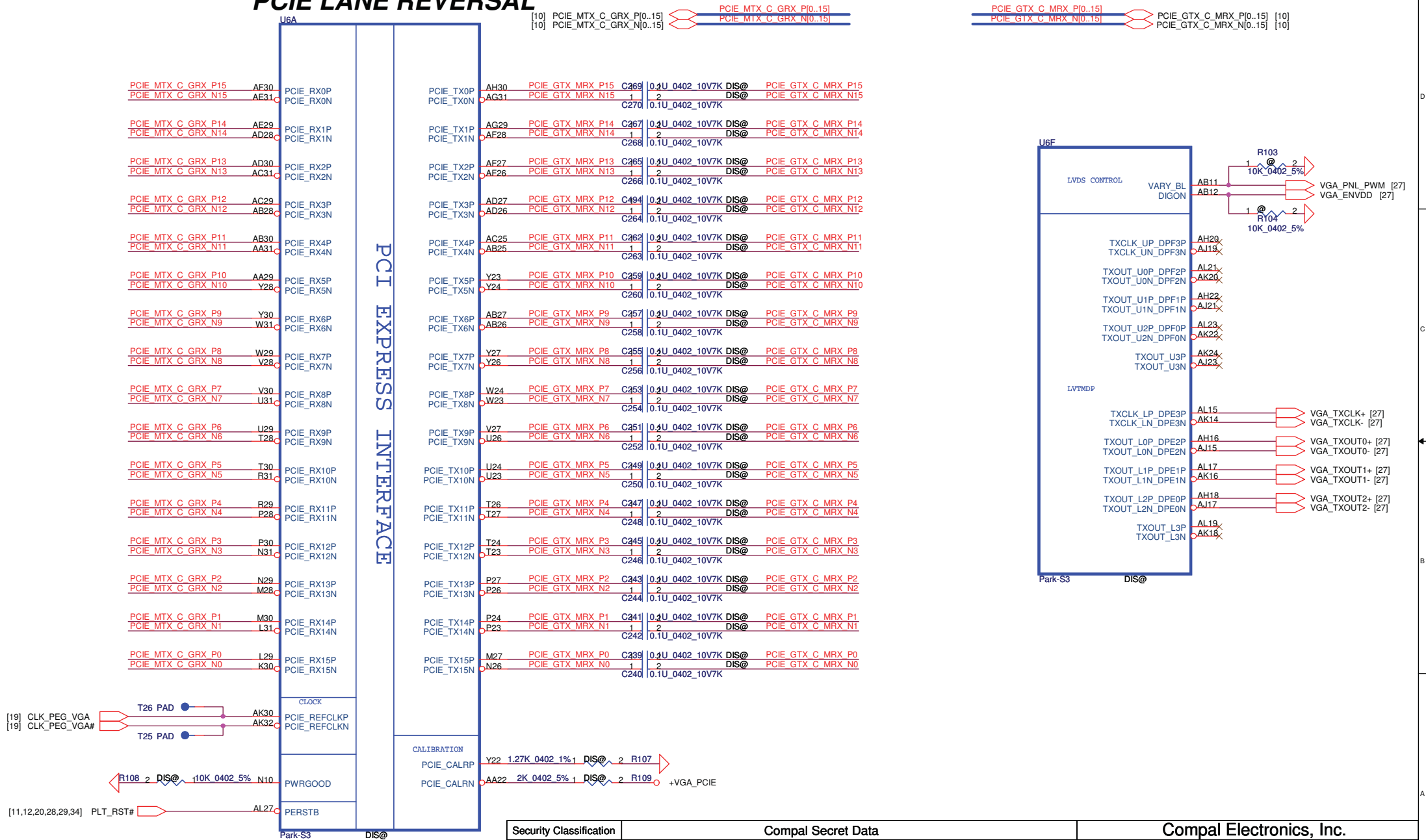
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# PCIE LANE REVERSAL



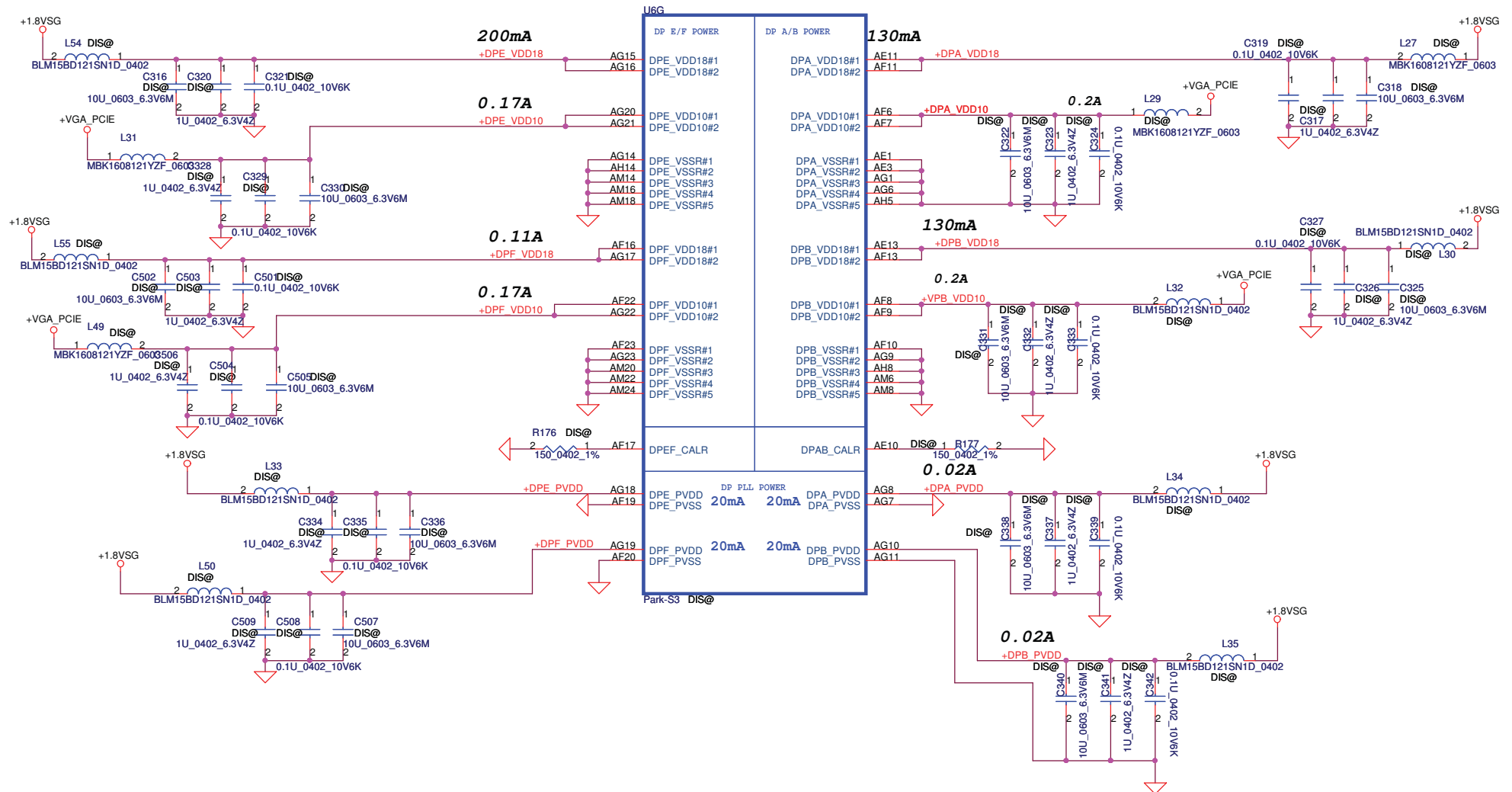








DPE\_VDD10  
DPF\_VDD10  
Park-S3: TMD5/DP=110mA@1.0V : LVDS=120mA@1.0V

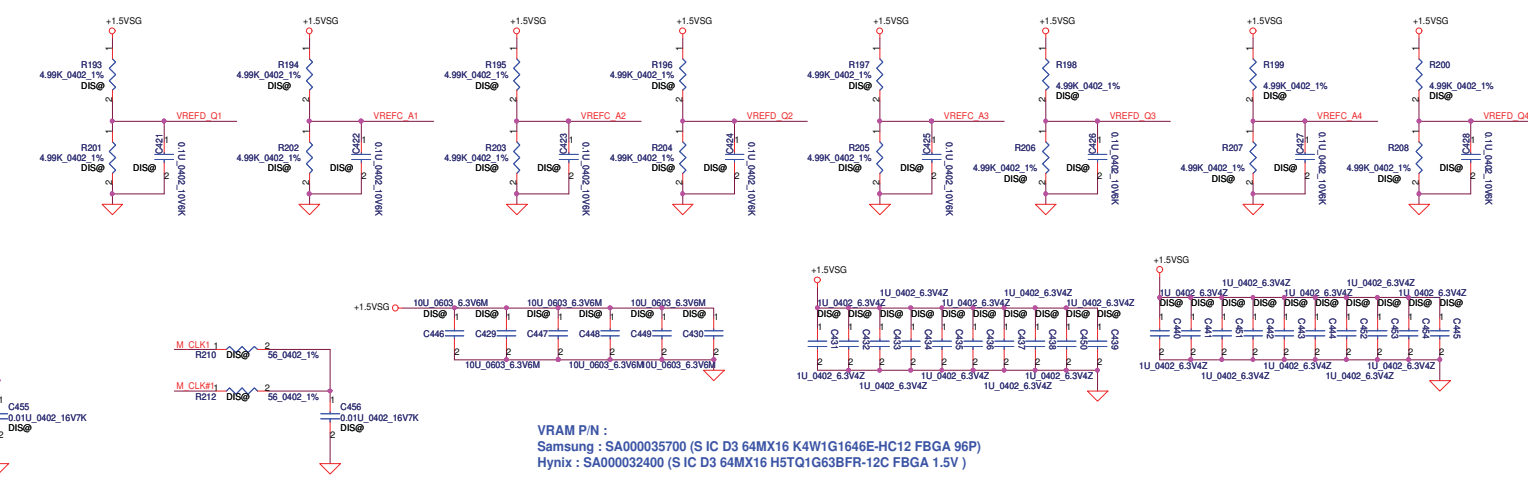
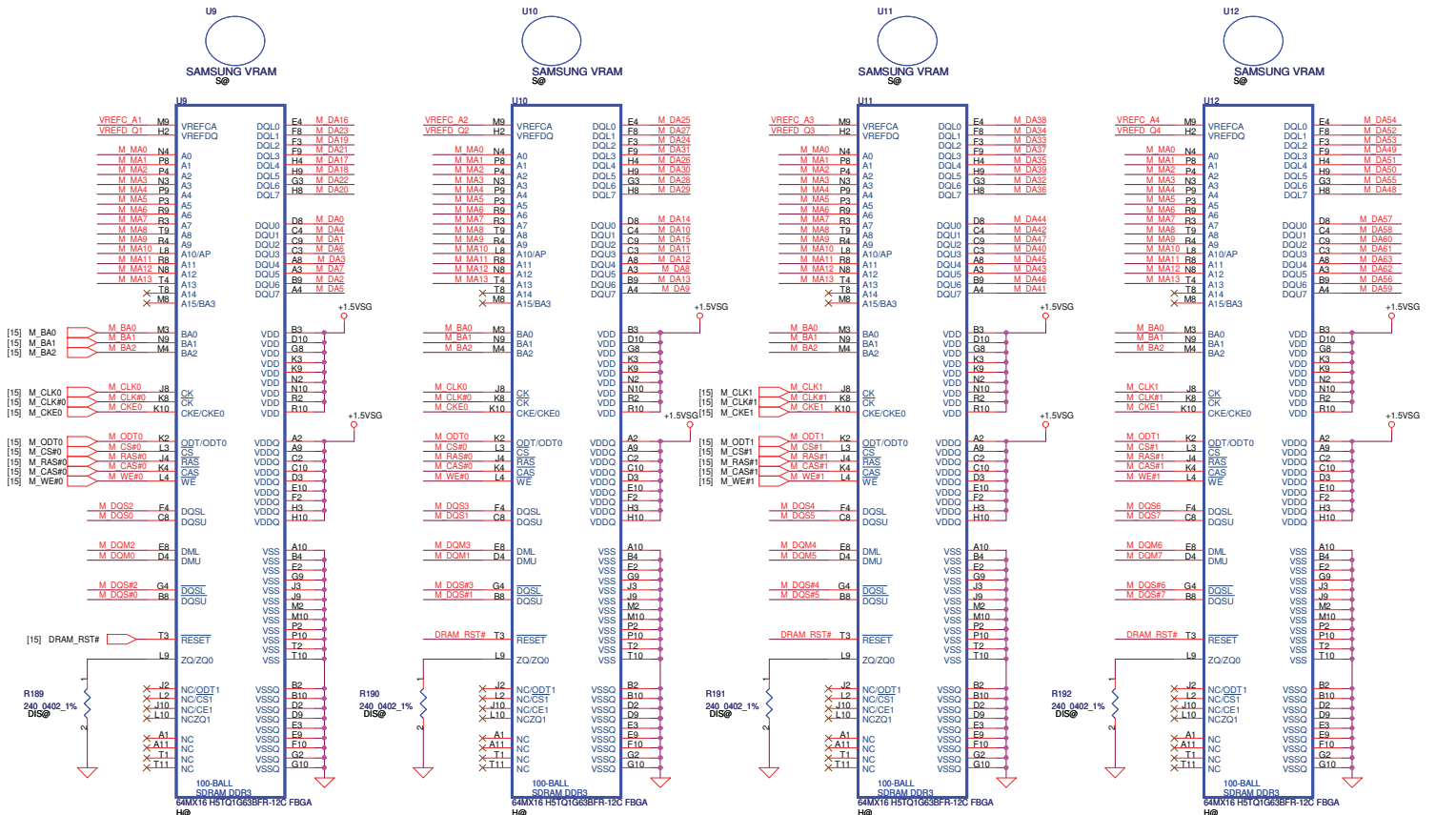


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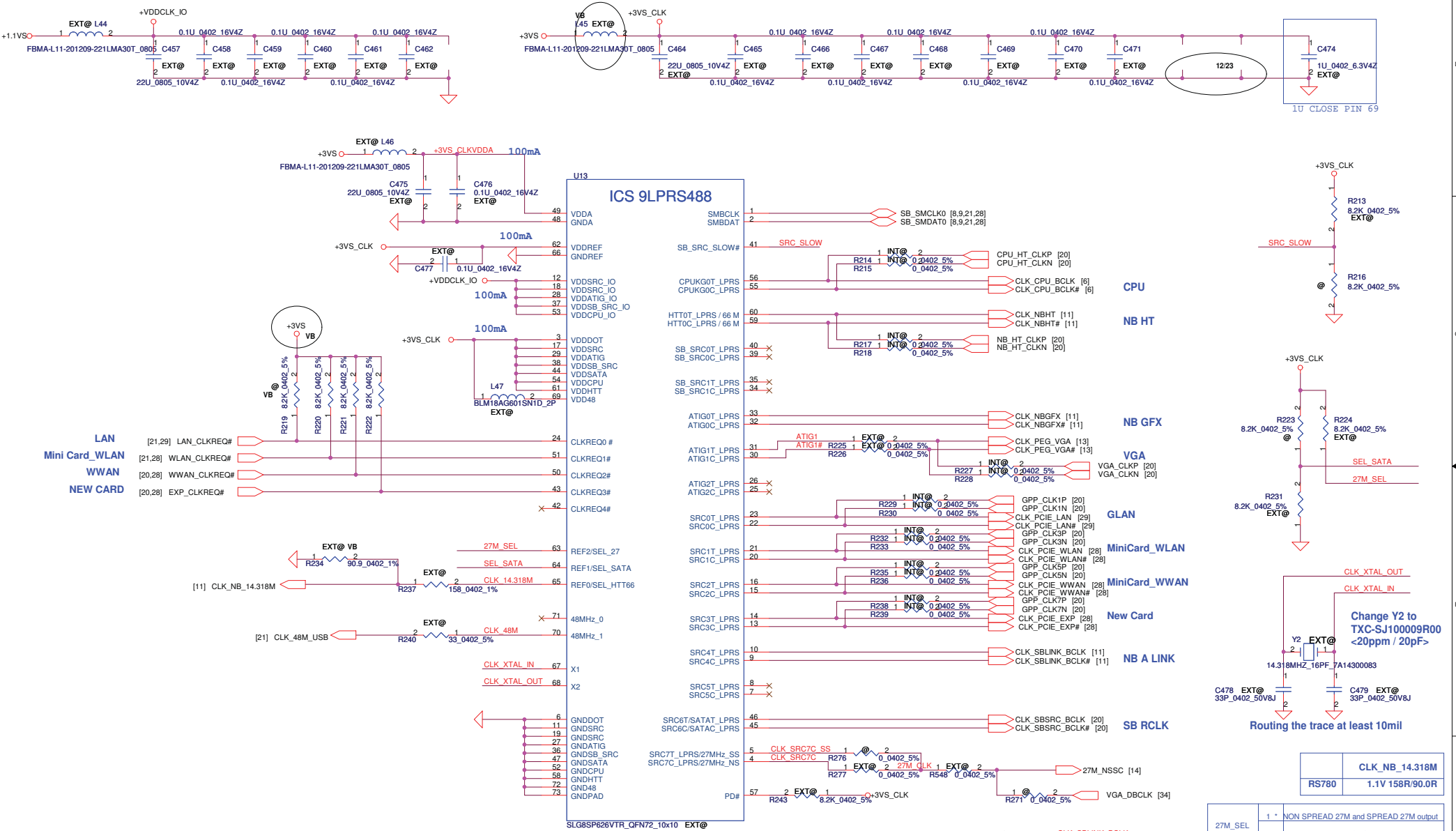
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VRAM P/N :  
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)  
 Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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Check Timing +1.1VS <50us +3VS for EXT CLKGEN satable



1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN  
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLTF MLF 72P CLK GEN

		CLK_NB_14.318M
	RS780	1.1V 158R/90.0R

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

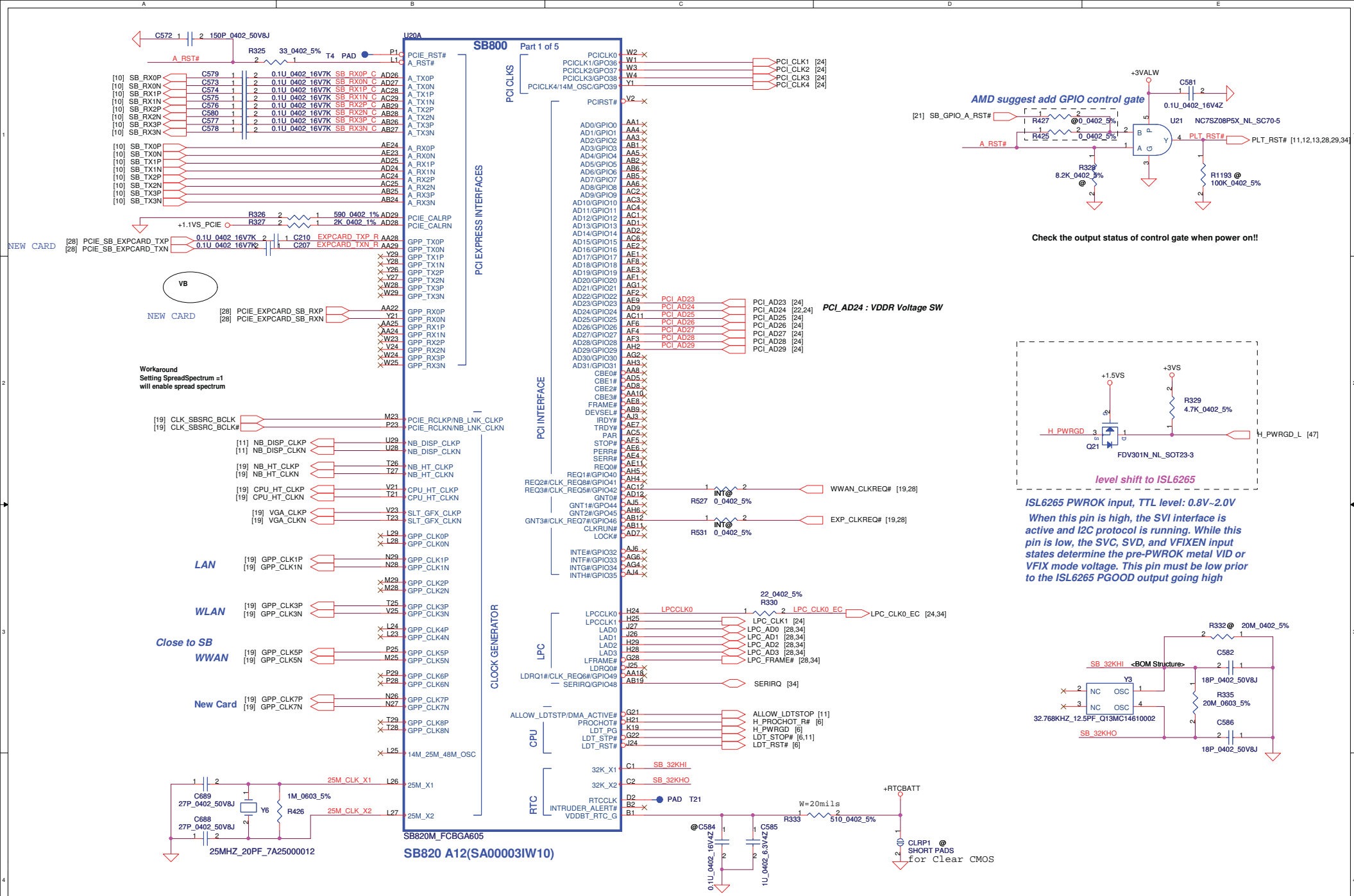
  

SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output

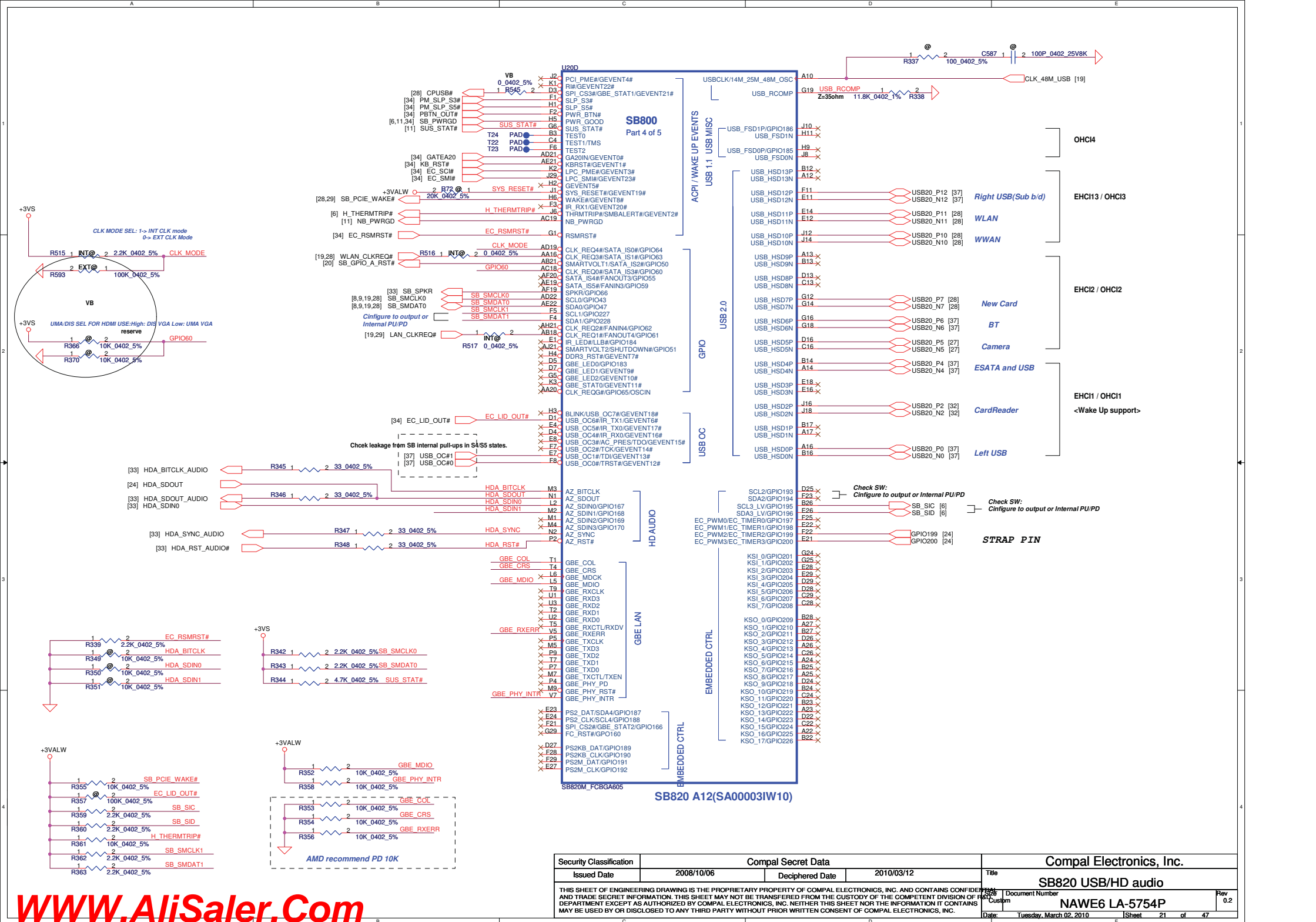
  

SEL_SATA	1	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

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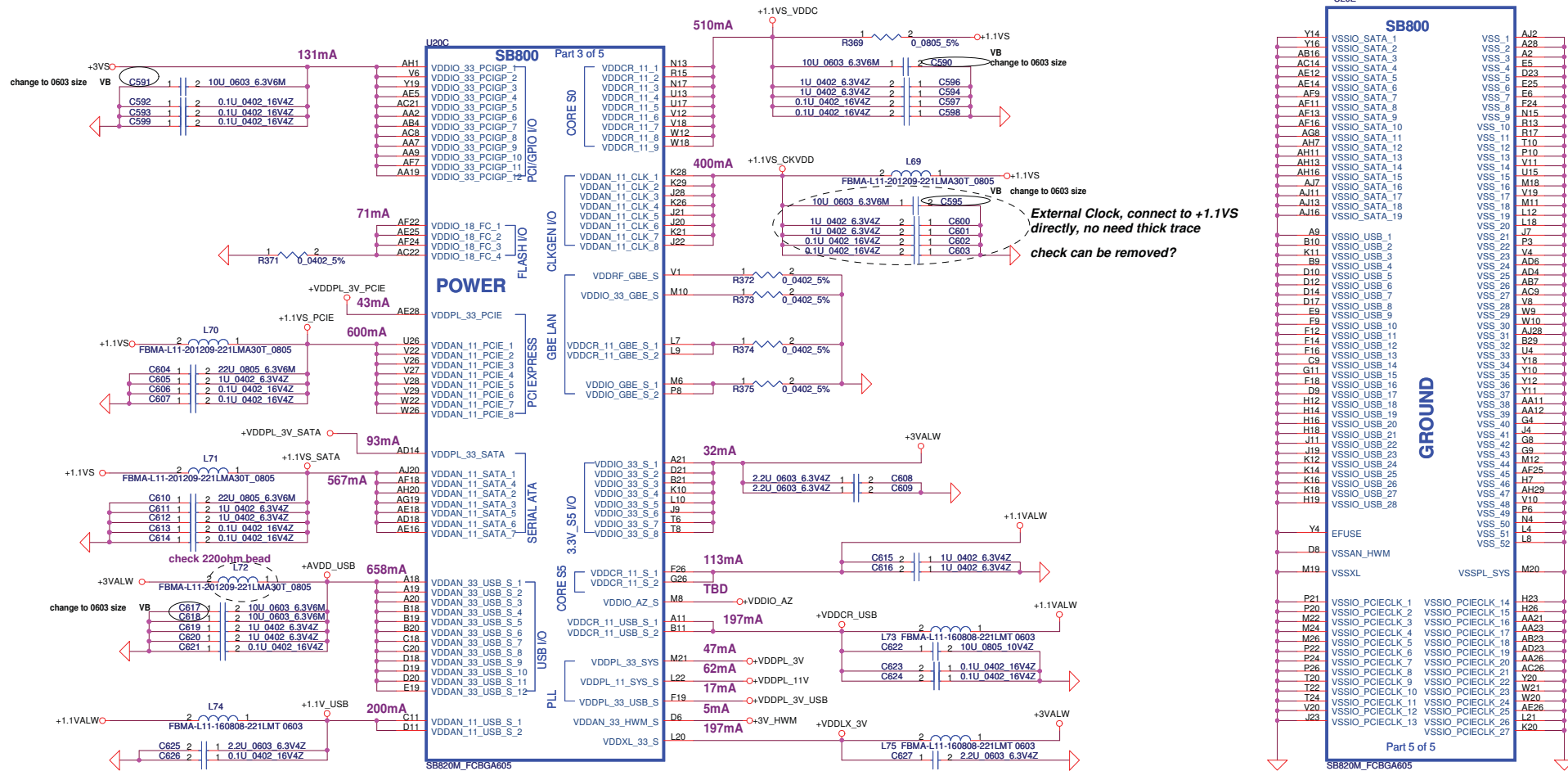
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								Document Number		NAWE6 LA-5754P	
								Date		Tuesday, March 02, 2010	
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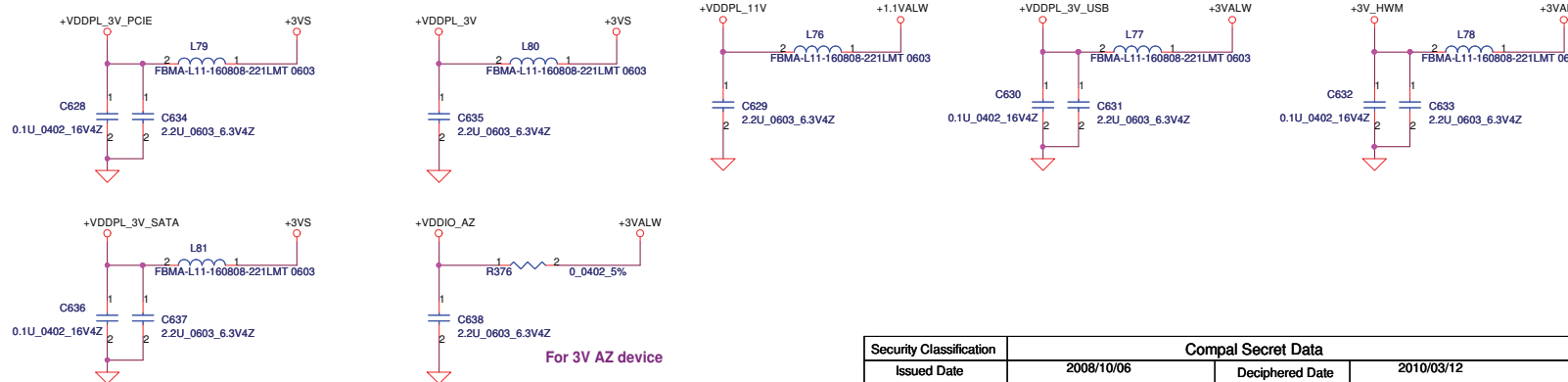






SB820 A12(SA00003IW10)

SB820 A12(SA00003IW10)



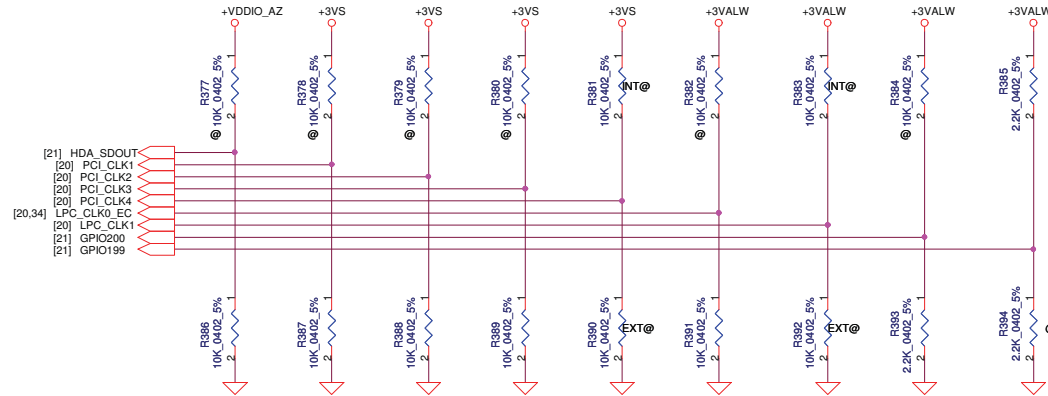
For 3V AZ device

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## REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
<b>PULL LOW</b>	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



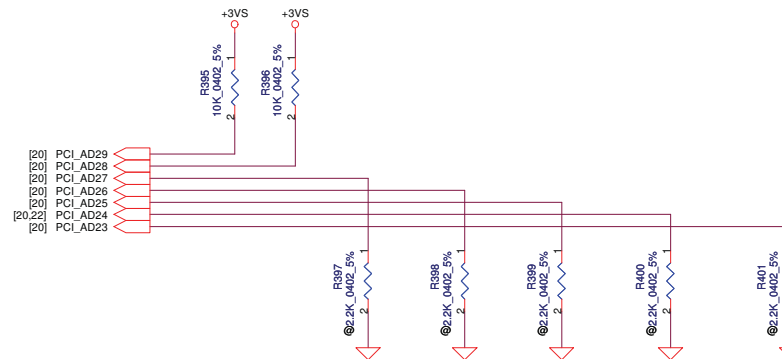
## DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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				SB820 STRAPS	0.2
				NAWE6 LA-5754P	
				Date: Monday, March 01, 2010	Sheet 24 of 47

# CRT Connector

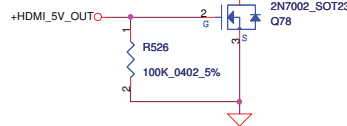
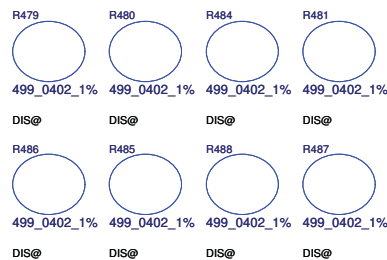
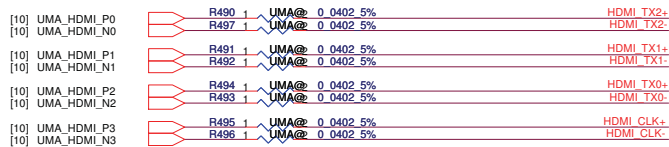
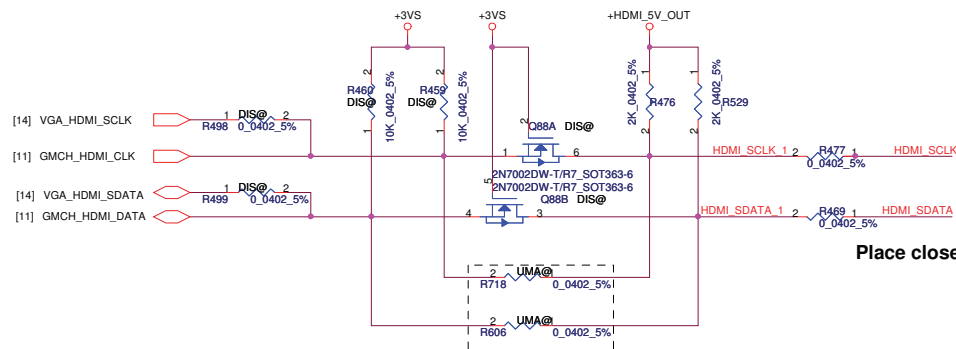
The schematic diagram illustrates the DSUB connector interface. It features two input signals, DSUB\_12 and DSUB\_15, which are connected to a network of resistors and two inverters. The resistors R457 and R553 are 4.7K\_0402\_5% and are connected to +CRT\_VCC. The resistors R676 and R544 are 0\_0402\_5% and are connected to +3VS. The inverters, DIS@ Q87A and DIS@ Q87B, are 2N7002DW-T/R7\_SOT363-6. The output of the first inverter is connected to CRT\_DATA, and the output of the second inverter is connected to CRT\_CLK.

Index	Label	Gene	Position	Strand	Score	Value	Value	Value	Value	Value
[1]	GMCH_CRT_R	GMCH CRT R	R677	2	UAA	1	0	0.402	5%	CRT_R
[1]	GMCH_CRT_G	GMCH CRT G	R542	2	UAA	1	0	0.402	5%	CRT_G
[1]	GMCH_CRT_B	GMCH CRT B	R679	2	UAA	1	0	0.402	5%	CRT_B
[11,12]	GMCH_CRT_HSYNC	GMCH CRT HSYNC	R547	2	UAA	1	0	0.402	5%	CRT_HSYNC
[11,12]	GMCH_CRT_VSYNC	GMCH CRT VSYNC	R543	2	UAA	1	0	0.402	5%	CRT_VSYNC
[11]	GMCH_CRT_DATA	GMCH CRT DATA	R546	2	UAA	1	0	0.402	5%	CRT_DATA
[11]	GMCH_CRT_CLK	GMCH CRT CLK	R678	2	UAA	1	0	0.402	5%	CRT_CLK

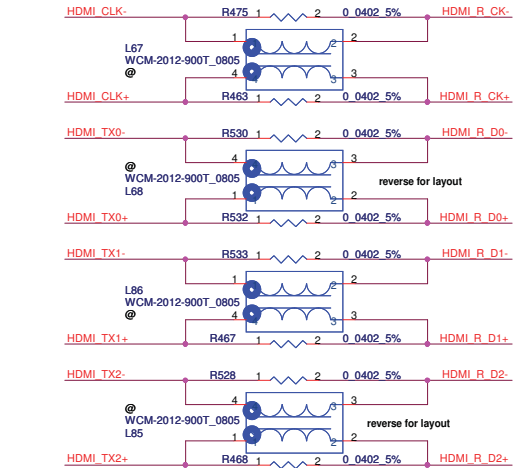
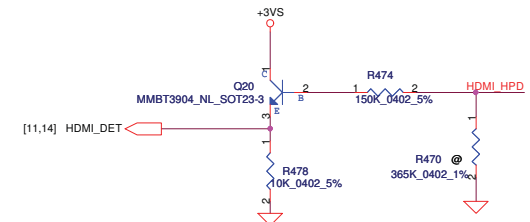
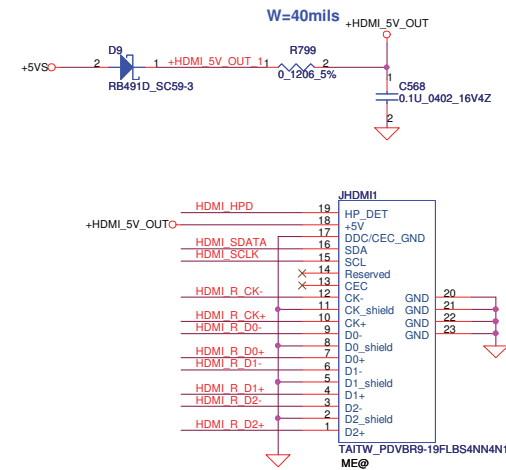
Device	Source	Target	Direction	Rate	Latency	Bandwidth	Frequency
[14]	VGA_CRT_R	VGA_CRT_R	R539	2	DISC	1	0.0402 5% CRT_R
[14]	VGA_CRT_G	VGA_CRT_G	R552	2	DISC	1	0.0402 5% CRT_G
[14]	VGA_CRT_B	VGA_CRT_B	R554	2	DISC	1	0.0402 5% CRT_B
[14]	VGA_CRT_HSYNC	VGA_CRT_HSYNC	R535	2	DISC	1	0.0402 5% CRT_HSYNC
[14]	VGA_CRT_VSYNC	VGA_CRT_VSYNC	R557	2	DISC	1	0.0402 5% CRT_VSYNC
[14]	VGA_CRT_DATA	VGA_CRT_DATA	R538	2	DISC	1	0.0402 5% CRT_DATA
[14]	VGA_CRT_CLK	VGA_CRT_CLK	R556	2	DISC	1	0.0402 5% CRT_CLK

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UMA use 715 ohm  
VGA use 499 ohm



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Date				Monday, March 01, 2010				Rev			
0.2				26				47			

[illegible][illegible]

VB

[34] INVT\_PWM → INVT\_PWM

[13] VGA\_PNL\_PWM → VGA\_PNL\_PWM

[11] GMCH\_INVT\_PWM → GMCH\_INVT\_PWM

1 0.0402\_5%

2 0.0402\_5%

R451 R452 R450 R442 10K\_0402\_5%

0

TXCLK+ TXCLK+	DIS@ 1	R466	2	0	0402	5%	VGA_TXCLK+ [13]
	DIS@ 1	R508	2	0	0402	5%	VGA_TXCLK+ [13]
TXOUT2+ TXOUT2+	DIS@ 1	R510	2	0	0402	5%	VGA_TXOUT2+ [13]
	DIS@ 1	R512	2	0	0402	5%	VGA_TXOUT2+ [13]
TXOUT1+ TXOUT1+	DIS@ 1	R511	2	0	0402	5%	VGA_TXOUT1+ [13]
	DIS@ 1	R512	2	0	0402	5%	VGA_TXOUT1+ [13]
TXOUT0+ TXOUT0+	DIS@ 1	R513	2	0	0402	5%	VGA_TXOUT0+ [13]
	DIS@ 1	R514	2	0	0402	5%	VGA_TXOUT0+ [13]
I2CC_SCL I2CC_SCL	DIS@ 2	R455	1	0	0402	5%	VGA_LCD_CLK [14]
	DIS@ 2	R441	1	0	0402	5%	VGA_LCD_DAT [14]

TXCLK	UMA@	R521	2	0	0402	5%		GMCH_TXCLKL [1]
TXCLK+	UMA@	R522	2	0	0402	5%		GMCH_TXCLKL [1]
TXOUT2-	UMA@	R556	2	0	0402	5%		GMCH_TXOUT2- [1]
TXOUT2+	UMA@	R557	2	0	0402	5%		GMCH_TXOUT2+ [1]
TXOUT1+	UMA@	R603	2	0	0402	5%		GMCH_TXOUT1+ [1]
TXOUT1-	UMA@	R604	2	0	0402	5%		GMCH_TXOUT1- [1]
TXOUT0+	UMA@	R602	2	0	0402	5%		GMCH_TXOUT0+ [1]
TXOUT0-	UMA@	R601	2	0	0402	5%		GMCH_TXOUT0- [1]
I2CC_SCL	UMA@	R453	1	0	0402	5%		GMCH_LCD_CLK [1]
I2CC_SDA	UMA@	R454	1	0	0402	5%		GMCH_LCD_DATA [11]

[illegible]

[34] BKOFF#

D10  
CH751H-40PT\_SOD323-2

+3VS

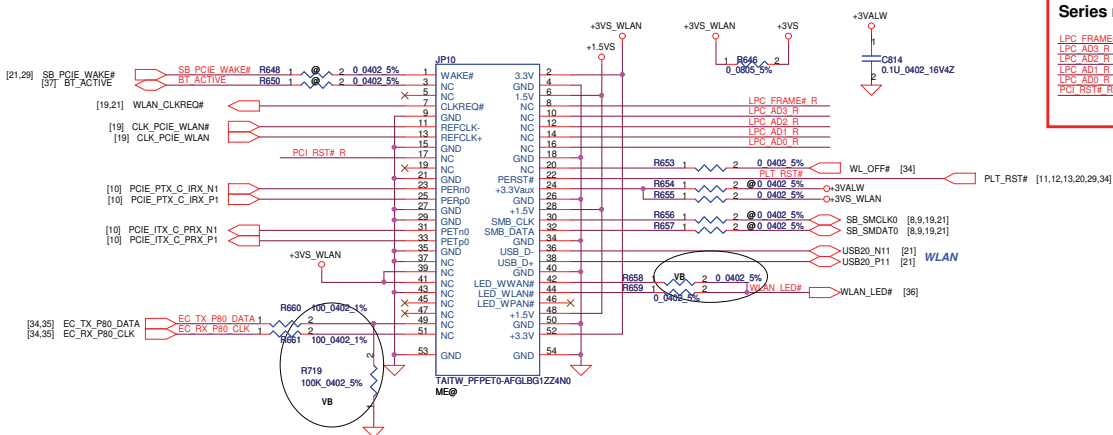
R429  
4.7K\_0402\_5%

R431  
10K\_0402\_3%

VB

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### Mini-Express Card for WLAN/WiMAX(Half)

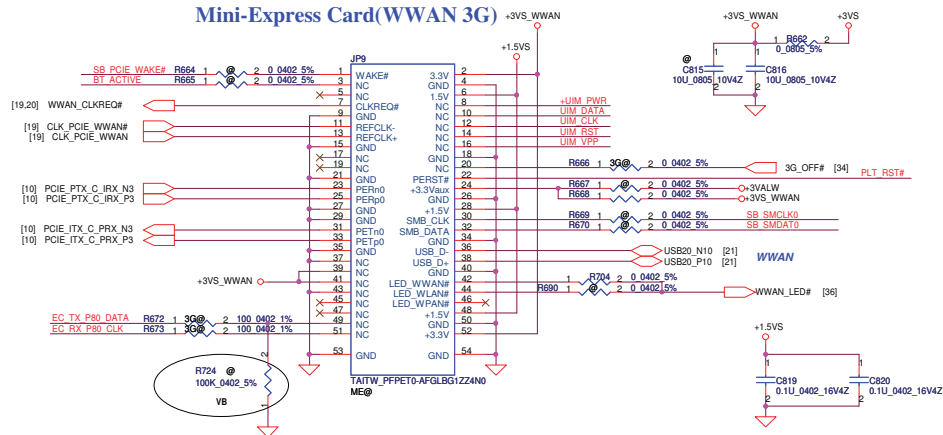


**Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.**

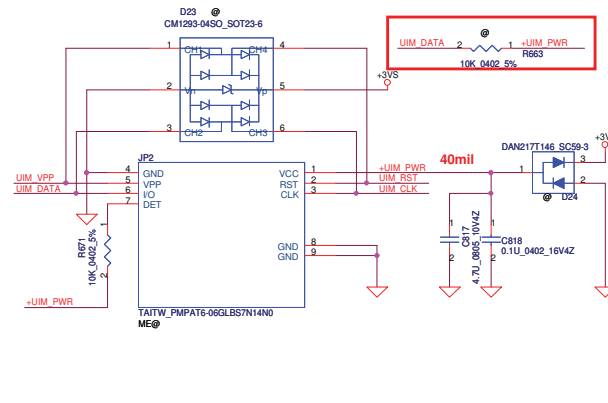
LPC FRAME# R	R644	1	2	0	0402 5%	LPC FRAME#	LPC FRAME# [20,34]
LPC AD3 R	R645	1	2	0	0402 5%	LPC AD3	LPC AD3 [20,34]
LPC AD2 R	R647	1	2	0	0402 5%	LPC AD2	LPC AD2 [20,34]
LPC AD1 R	R649	1	2	0	0402 5%	LPC AD1	LPC AD1 [20,34]
LPC AD0 R	R651	1	2	0	0402 5%	LPC AD0	LPC AD0 [20,34]
PLT RST# R	R652	1	2	0	0402 5%	PLT RST#	PLT RST# [11,12,13,20,34]

### Mini-Express Card for WWAN(Full)

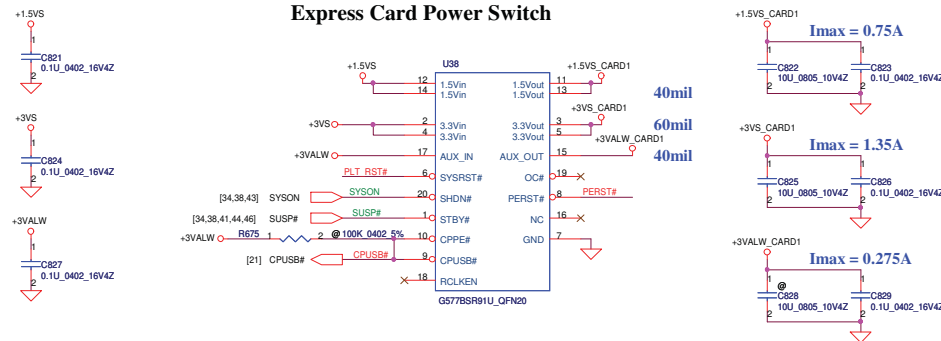
Mini-Express Card(WWAN 3G) +3VS\_WWAN



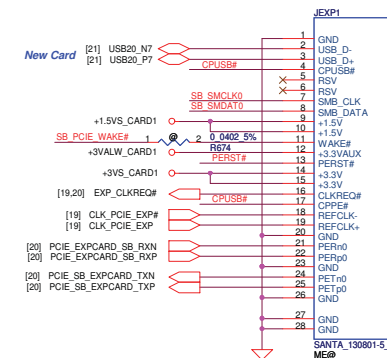
Vcc 3.3V +/- 8%  
Peak Icc 2750mA  
with max supply droop 50mA  
Average Icc 1000mA



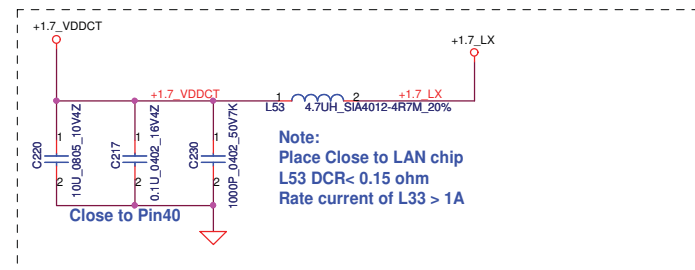
## Express Card Power Switch



***New Card 34mm Socket (Left/TOP)***



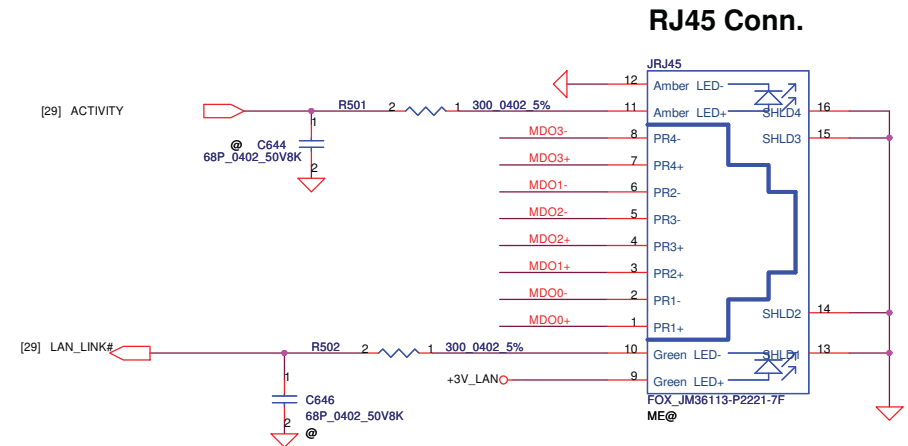
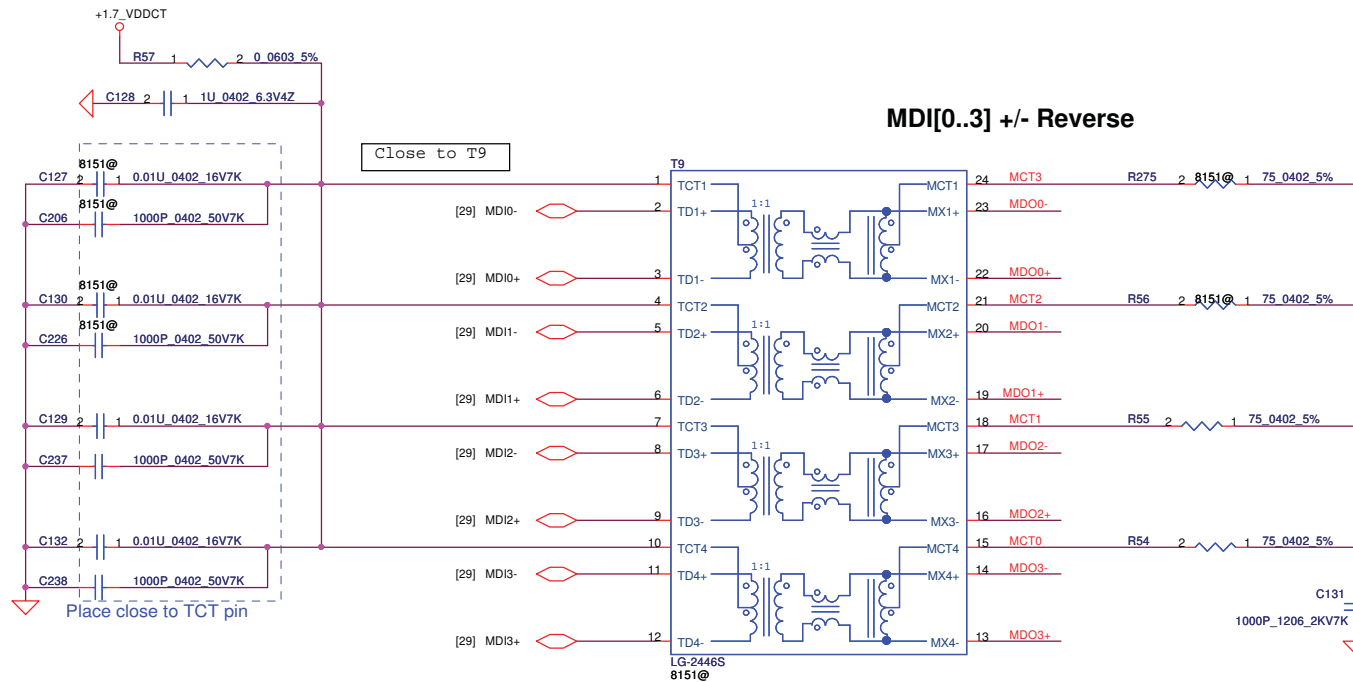
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>				
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						<b>Mini-Card/Nwe Card/SIM</b>		
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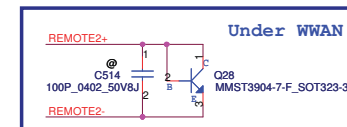
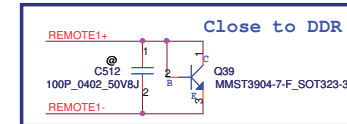
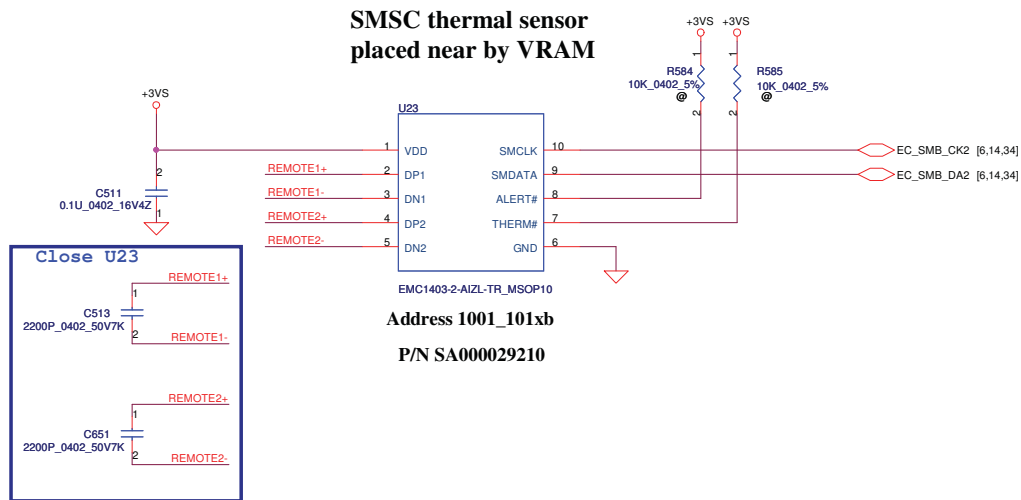
Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
	H:SWR Switch mode regulator Select *  AR8151 Pin23=LED2.  AR8152, Pin23 is CLKREQ	--

8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resister and cap

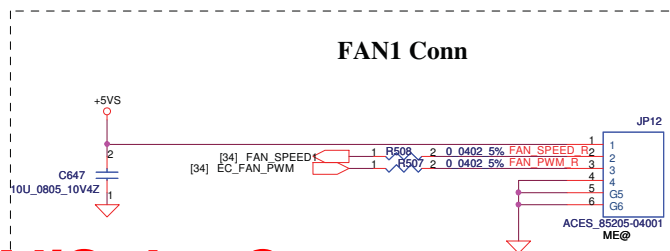




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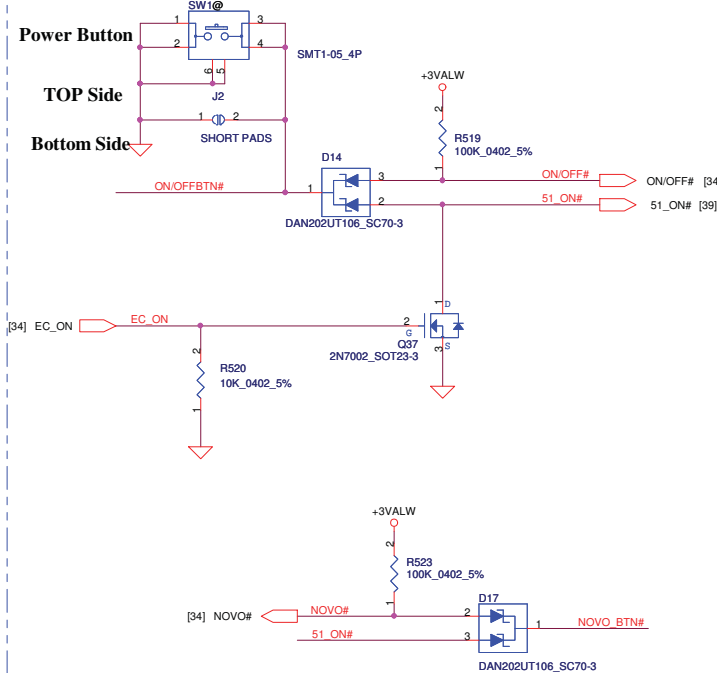


REMOTE1,2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

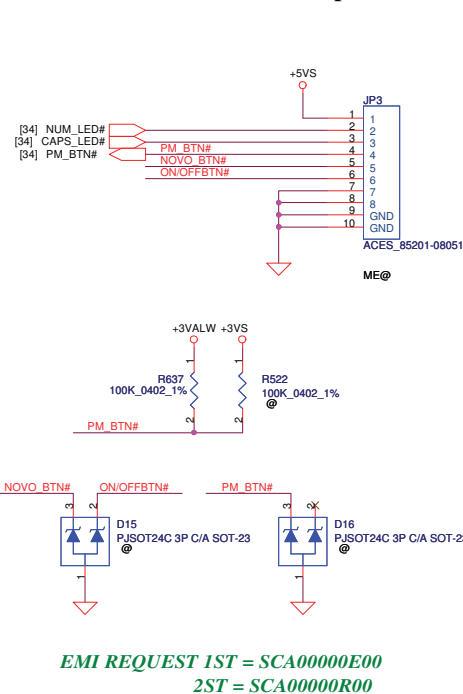


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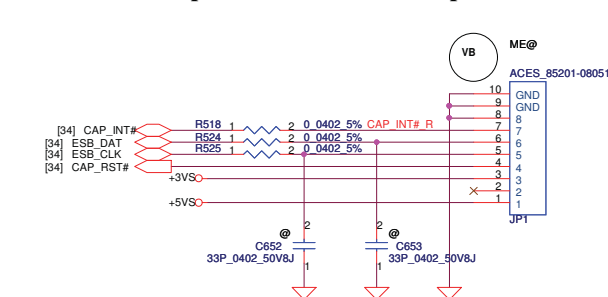
## ON/OFF switch



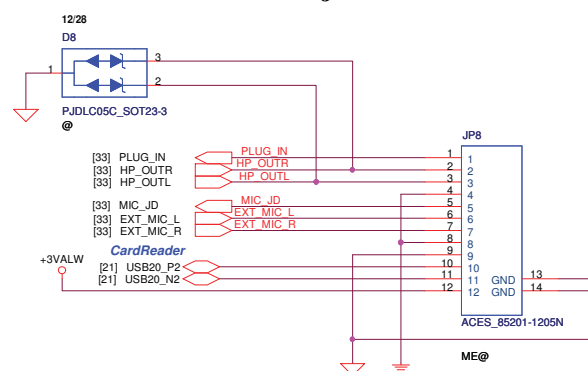
## Power Bottom Board Conn. 8pin



## Cap Sensor Board Conn. 8pin

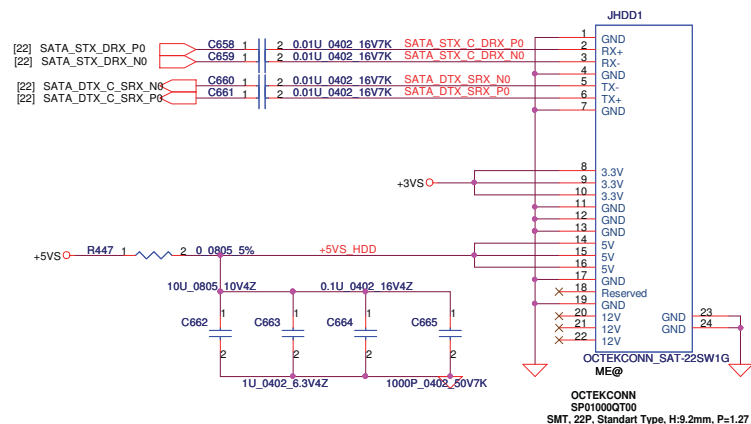
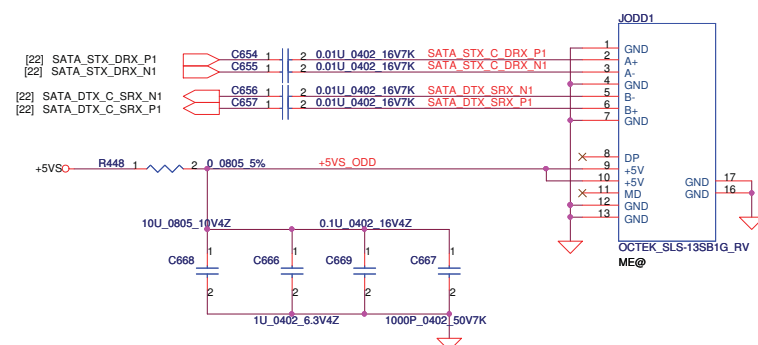


## Card Reader/Audio Jack SB CONN



## SATA HDD Conn.

## SATA ODD Conn.

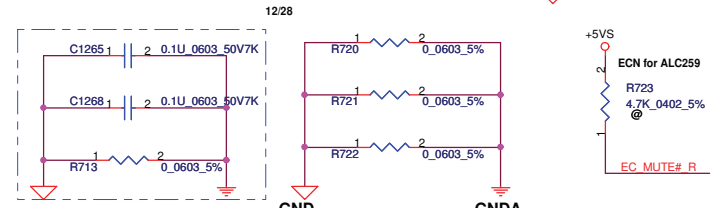
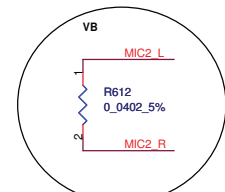
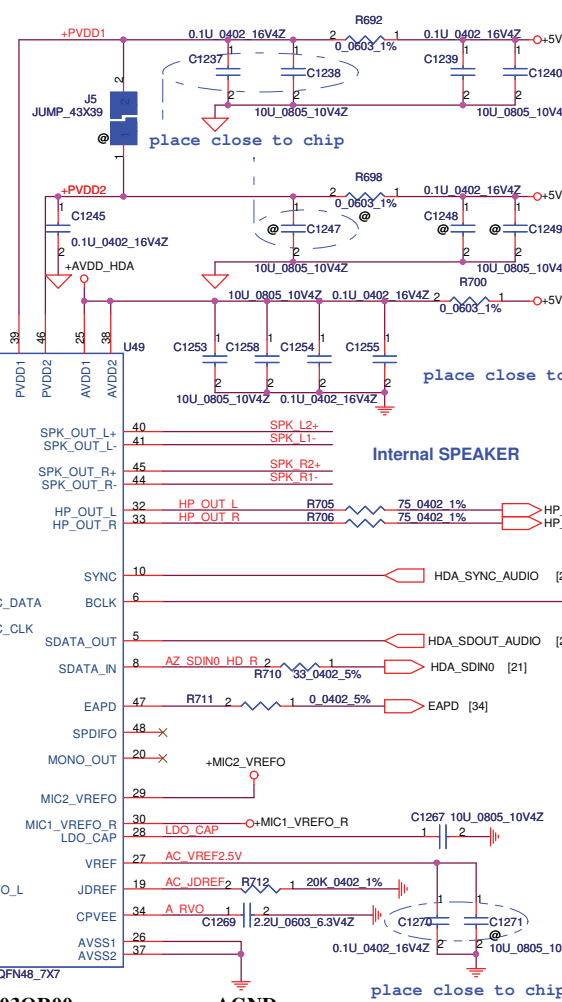
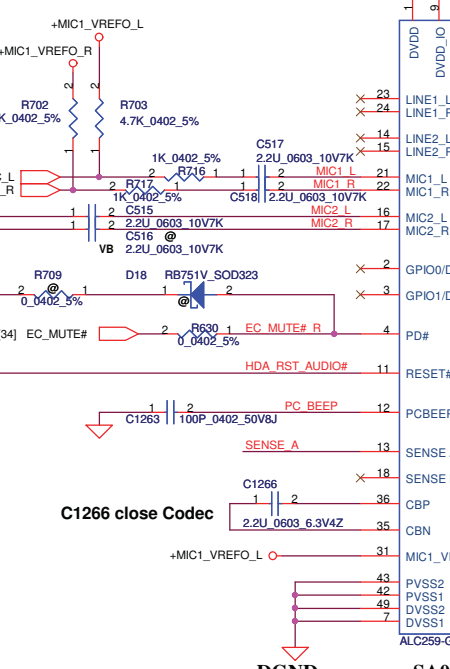
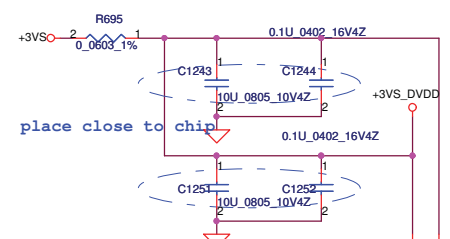


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[34] BEEP#

C1242  
1u\_0603\_10V4Z  
R696  
560\_0402\_5%  
Q86  
2SC2414KT145\_SOT23  
R697  
2.4K\_0402\_1%  
C1250

RB751V\_SOD323

[illegible][illegible]

SPK\_OUT\_R+ 45 SPK R2+  
SPK\_OUT\_R- 44 SPK R1-  
HP\_OUT\_L 32 HP OUT L R705 75 0402 1% HP  
HP\_OUT\_R 33 HP OUT R R706 75 0402 1% HP

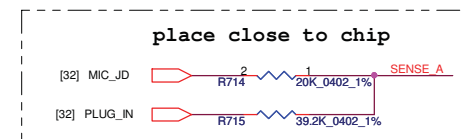
SYNC 10 HDA\_SYNC\_AUDIO [2]

BCLK 6

SDATA\_OUT 5 HDA\_SDOUT\_AUDIO [2]

For EMI

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	

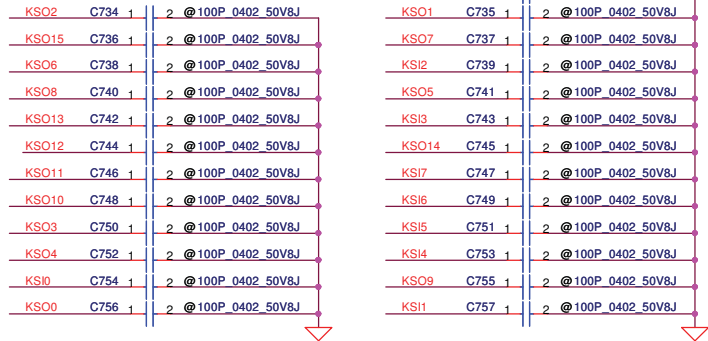


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				Size	Document Number
				Date	<b>NAWE6 LA-5754P</b>
				Date: <b>tuesday, March 02, 2010</b>	Sheet <b>33</b> of <b>47</b>



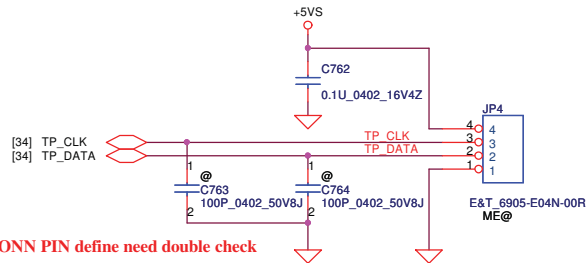
## INT\_KBD Conn.

KSI[0..7] KSI[0..7] [34]  
KSO[0..17] KSO[0..17] [34]

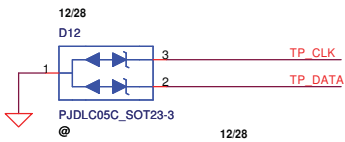


CONN PIN define need double check

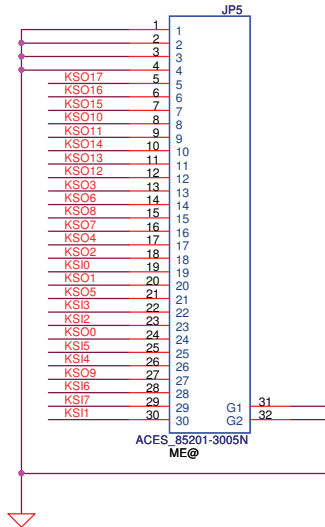
## To TP/B Conn.



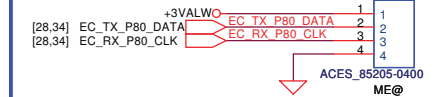
CONN PIN define need double check



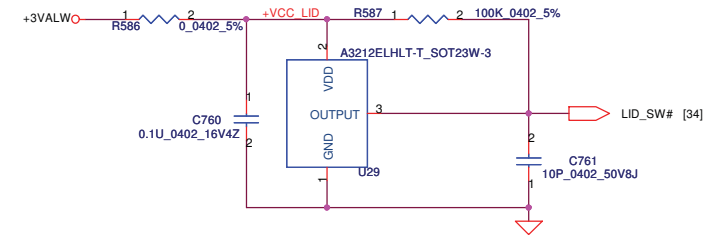
## reversal of NIWE1



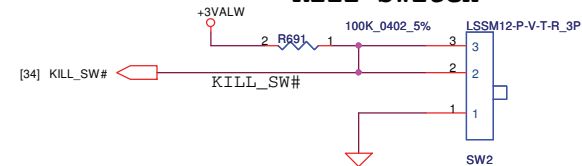
## EC DEBUG PORT



## Lid Switch



## Kill Switch

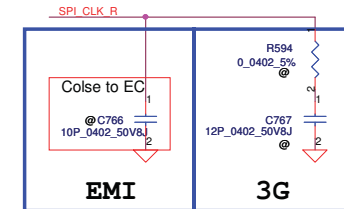
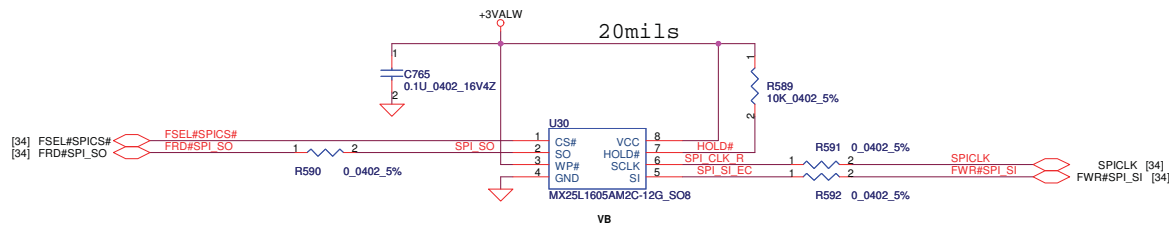


## Kill

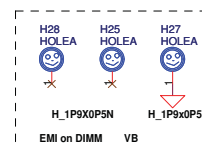
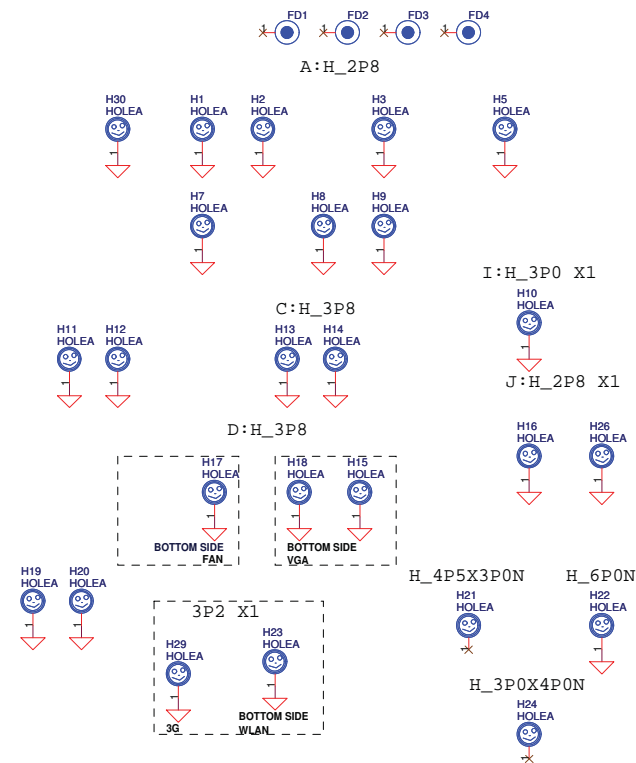
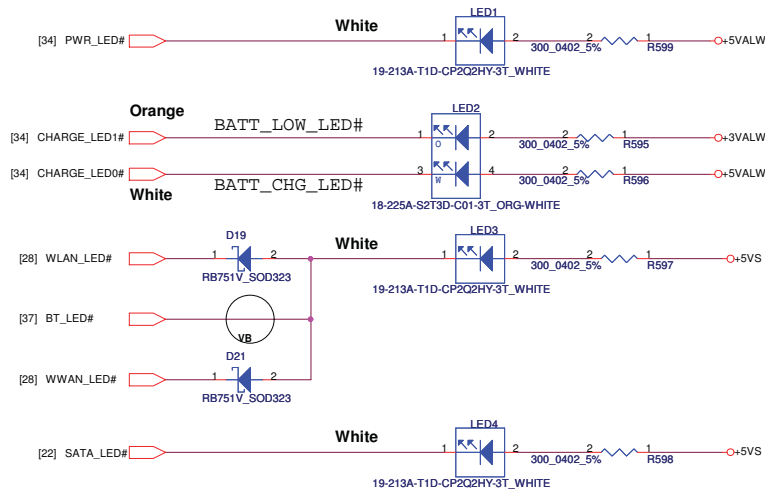
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Date	Monday, March 01, 2010	Sheet	35	of 47

SA00002TO00 package 200mil  
S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM



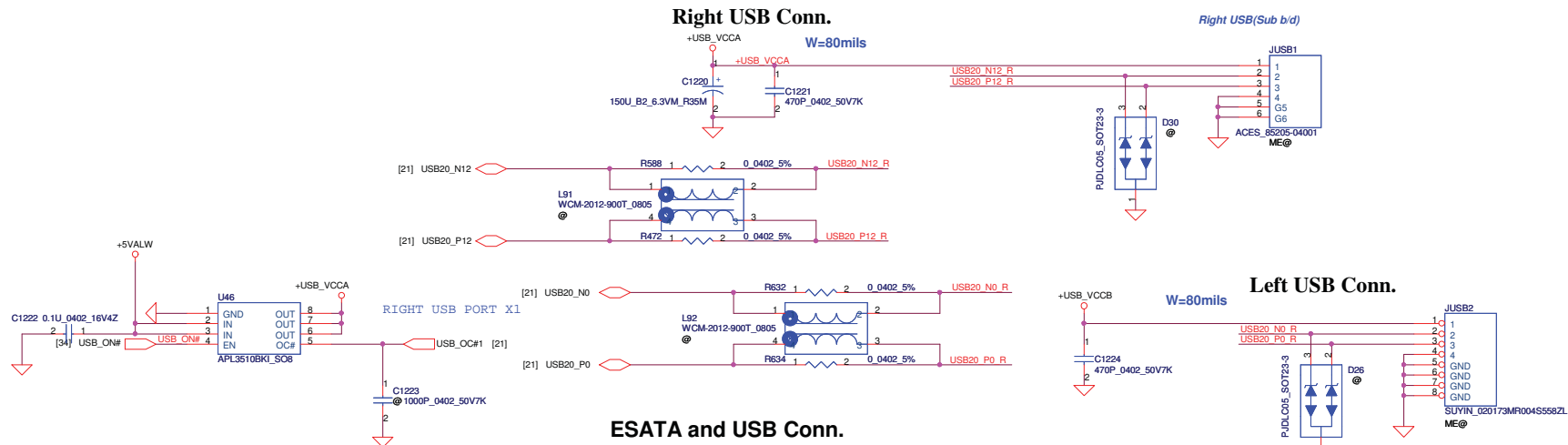
**LED**



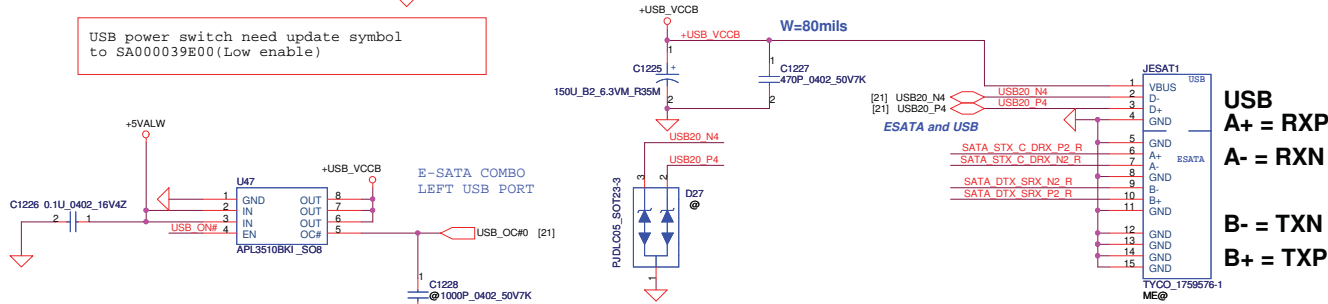
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>LED/EC SPI ROM</b>	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Document Number	NAWE6 LA-5754P
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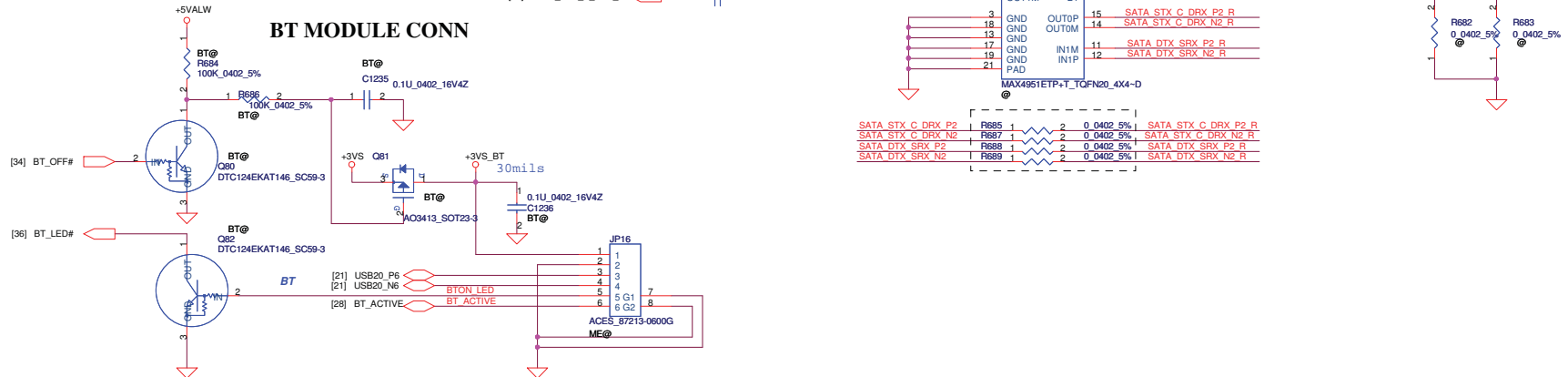
## Right USB Conn.



## ESATA and USB Conn.

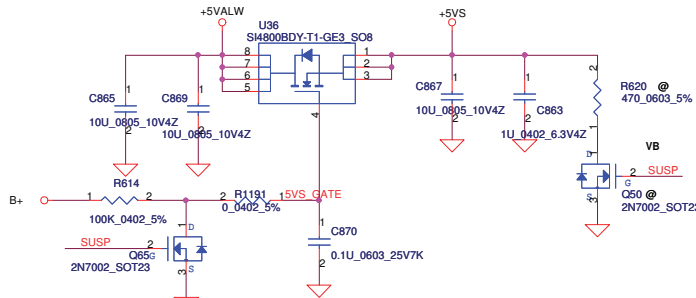


## BT MODULE CONN

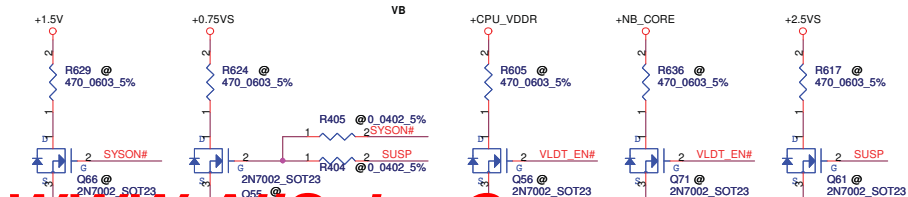
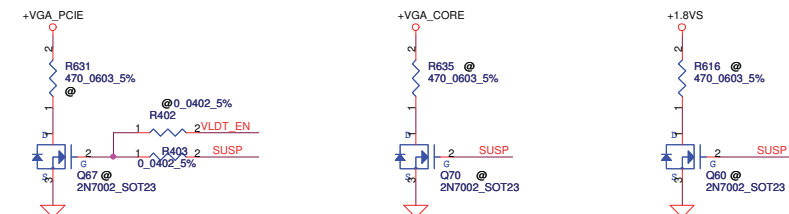
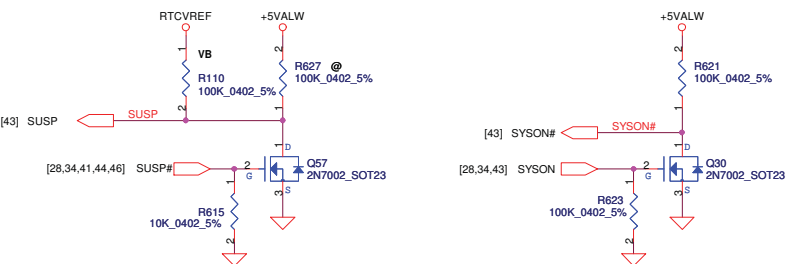
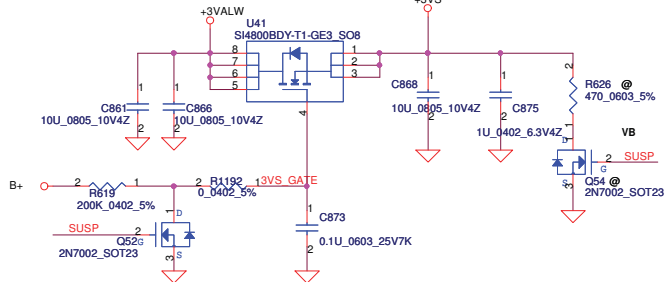


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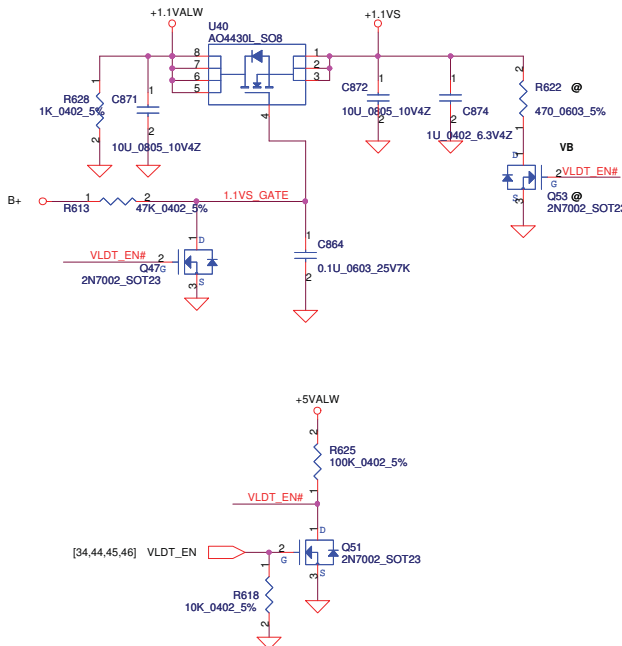
### +5VALW TO +5VS



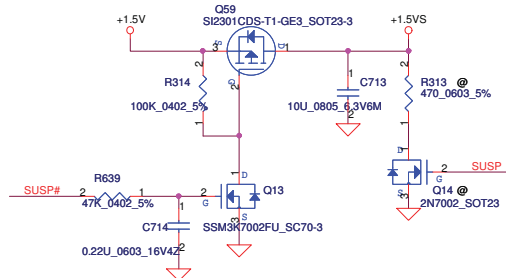
### +3VALW TO +3VS



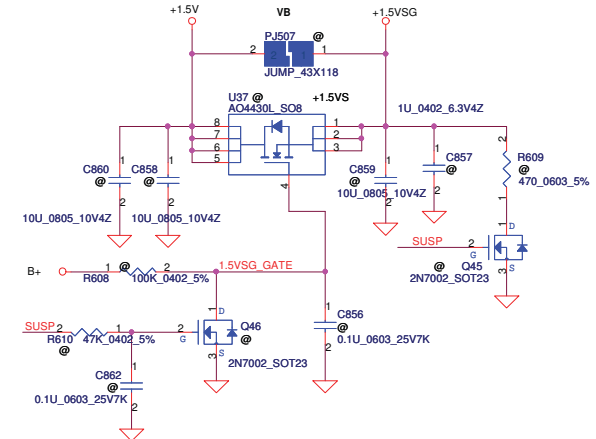
### +1.1VALW TO +1.1VS (NB HT)



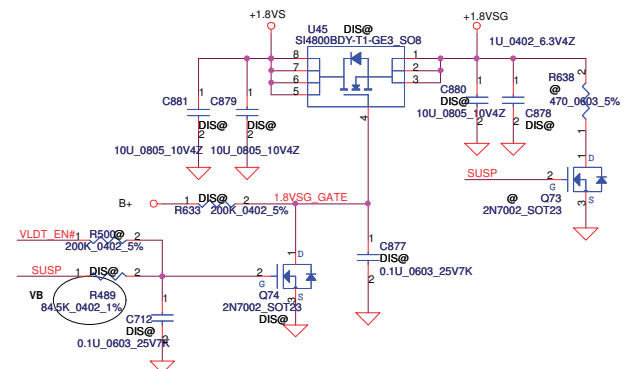
### +1.5VS



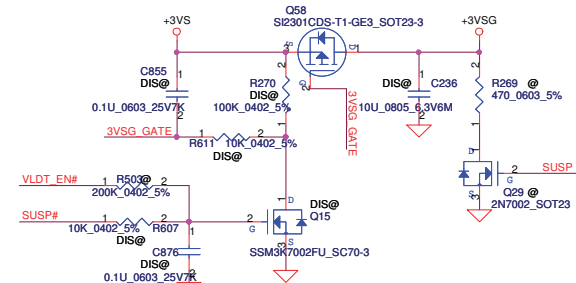
### +1.5V to +1.5VSG



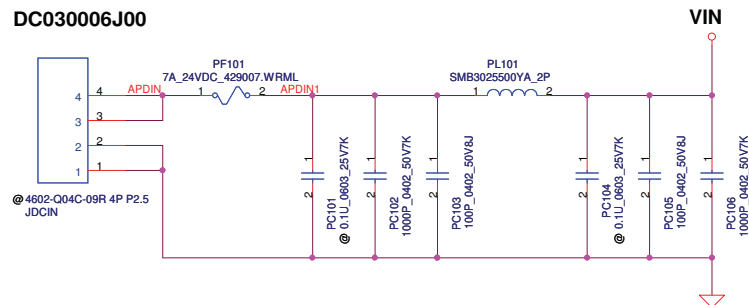
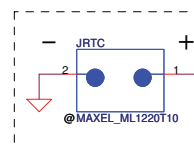
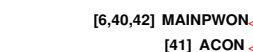
### +1.8VS to +1.8VSG



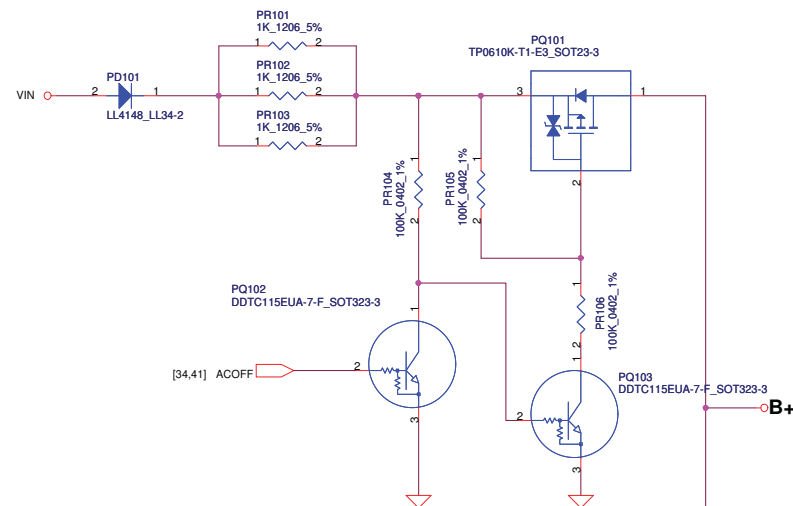
### +3VSG



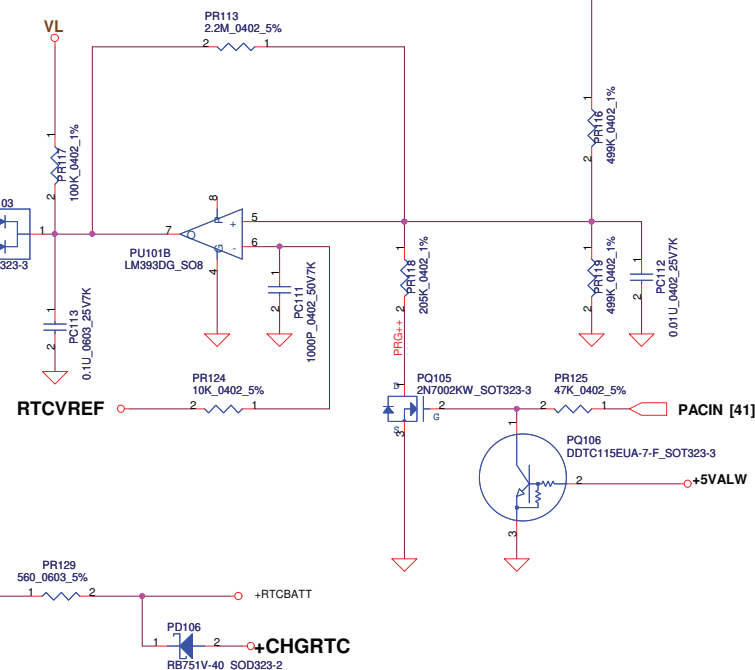
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Issued Date	2008/10/06	Deciphered Date	2010/03/12	DC Interface	
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				Date	Tuesday, March 02, 2010
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[illegible]

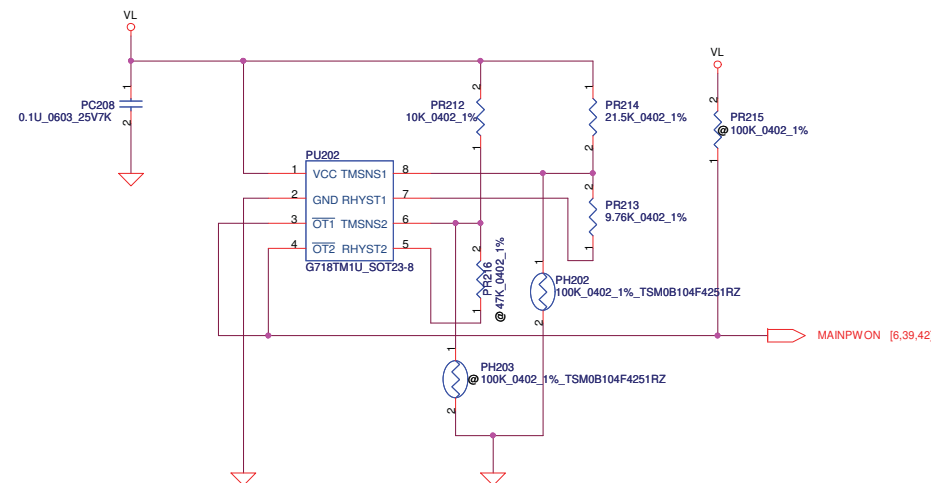
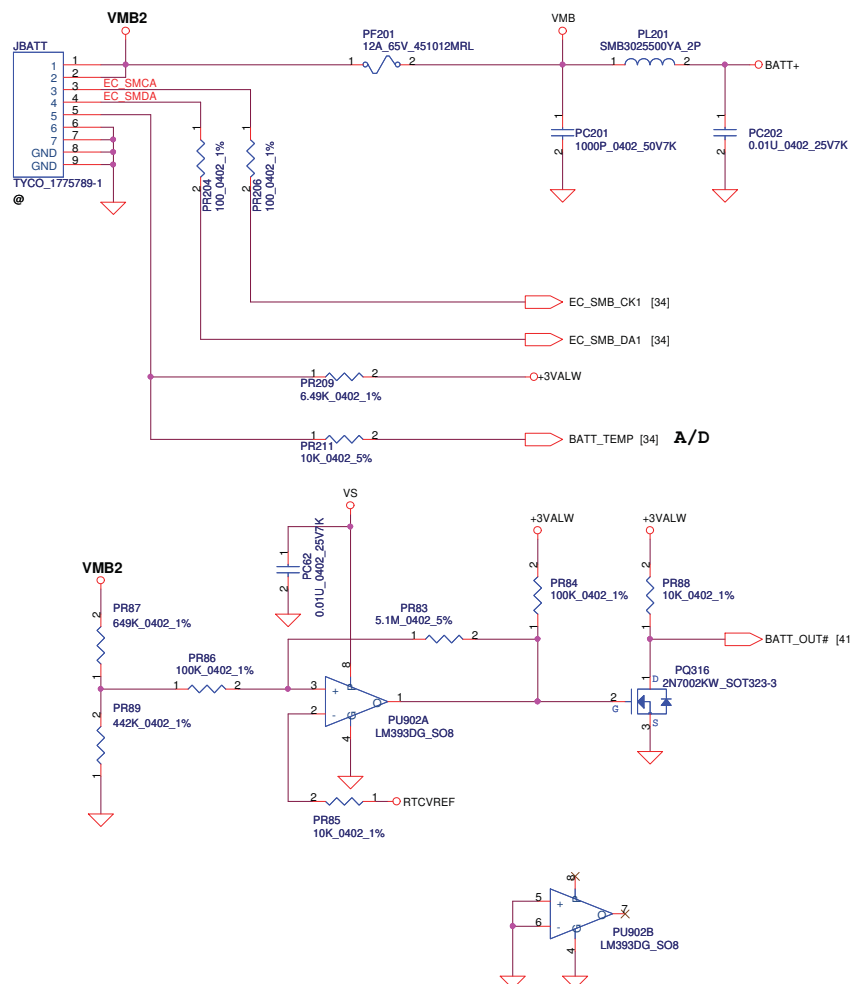
	Min.	typ.	Max
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V



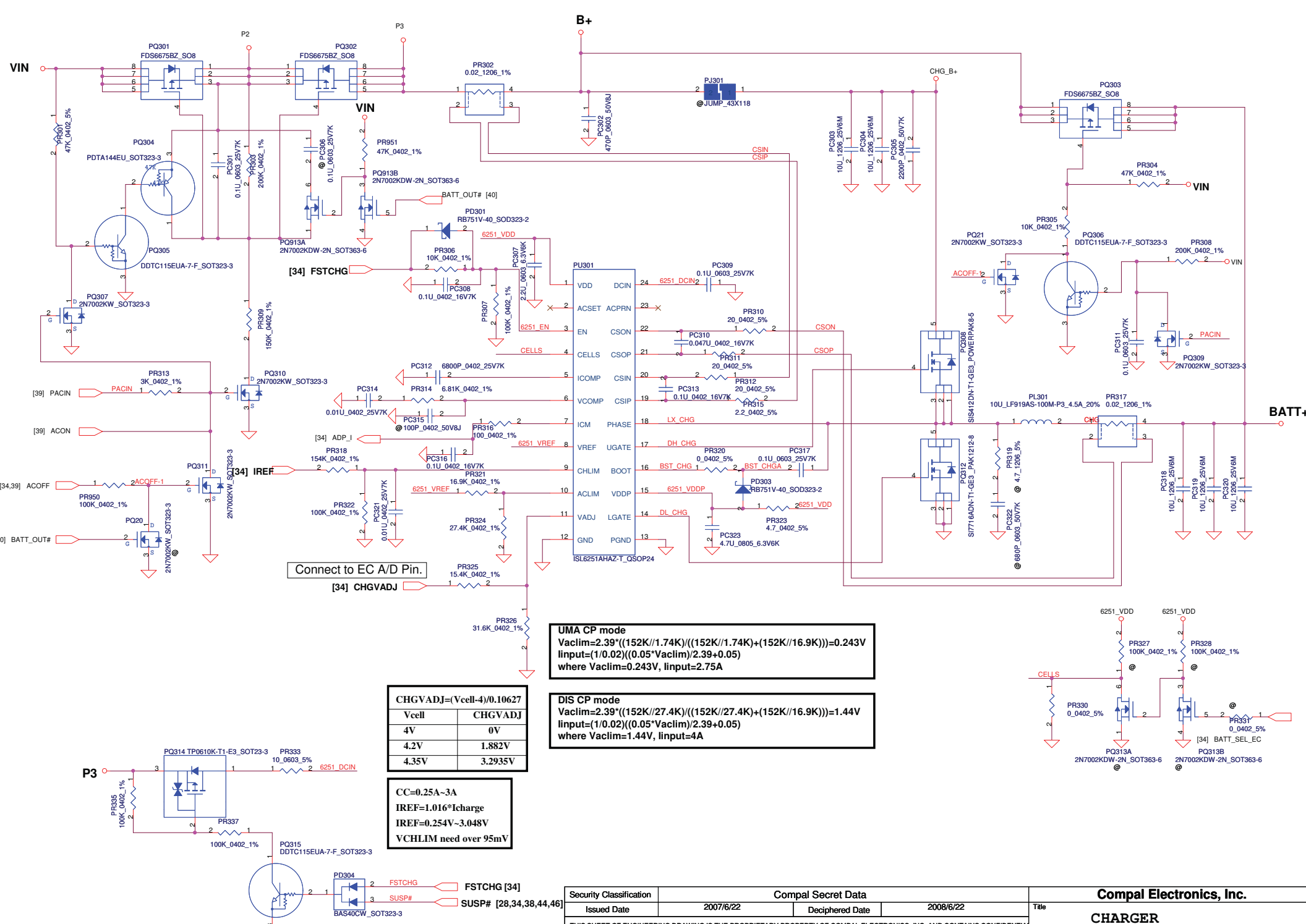
	Min.	typ.	Max
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



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Connect to EC A/D Pin.

[34] CHGVADJ

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A  
IREF=1.016\*Icharge  
IREF=0.254V~3.048V  
VCHLIM need over 95mV

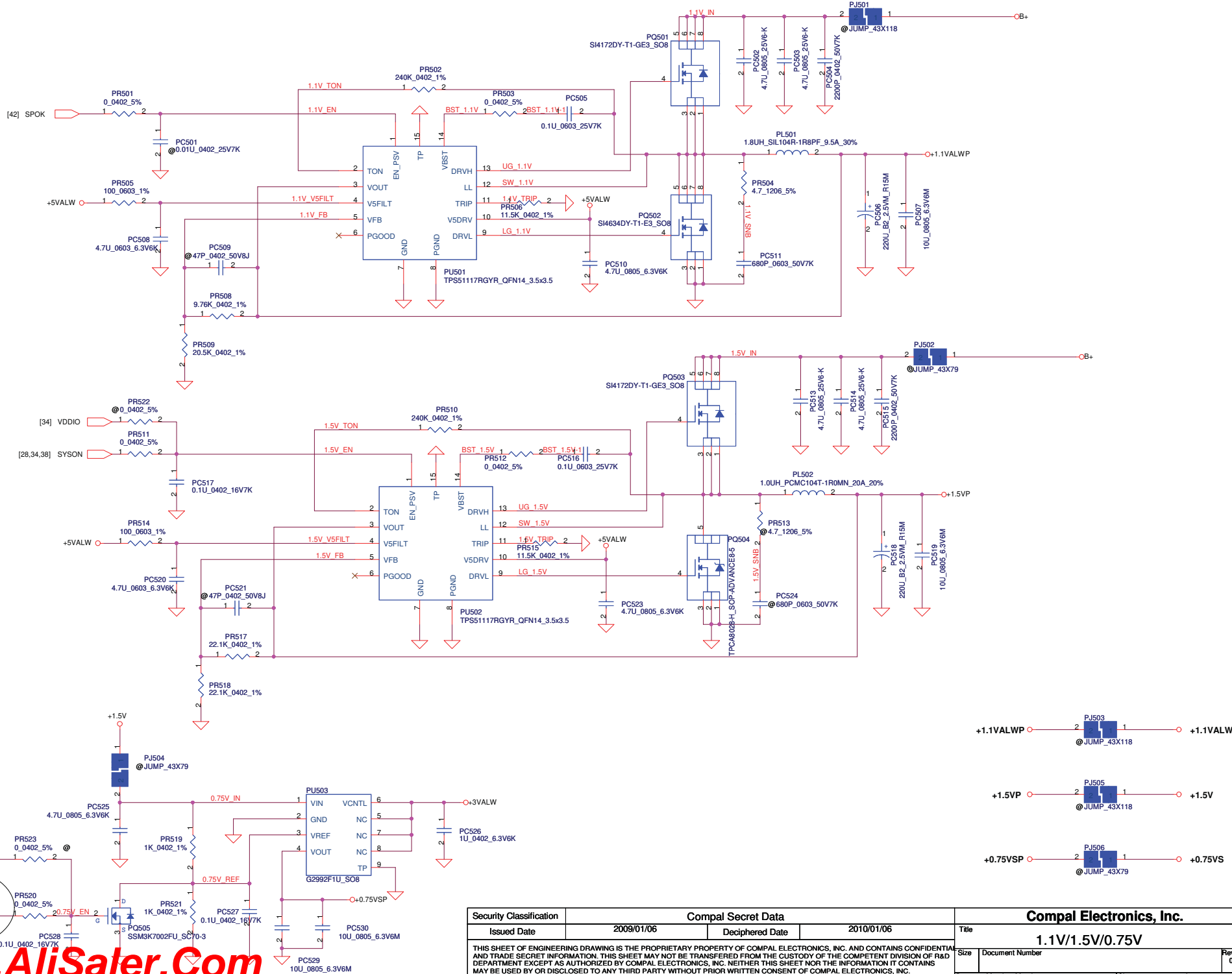
UMA CP mode  
 $V_{acli} = 2.39 * ((152K / 1.74K) / ((152K / 1.74K) + (152K / 16.9K))) = 0.243V$   
 $I_{in} = (1 / 0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$   
where  $V_{acli} = 0.243V$ ,  $I_{in} = 2.75A$

DIS CP mode  
 $V_{acli} = 2.39 * ((152K / 27.4K) / ((152K / 27.4K) + (152K / 16.9K))) = 1.44V$   
 $I_{in} = (1 / 0.02) * ((0.05 * V_{acli}) / 2.39 + 0.05)$   
where  $V_{acli} = 1.44V$ ,  $I_{in} = 4A$

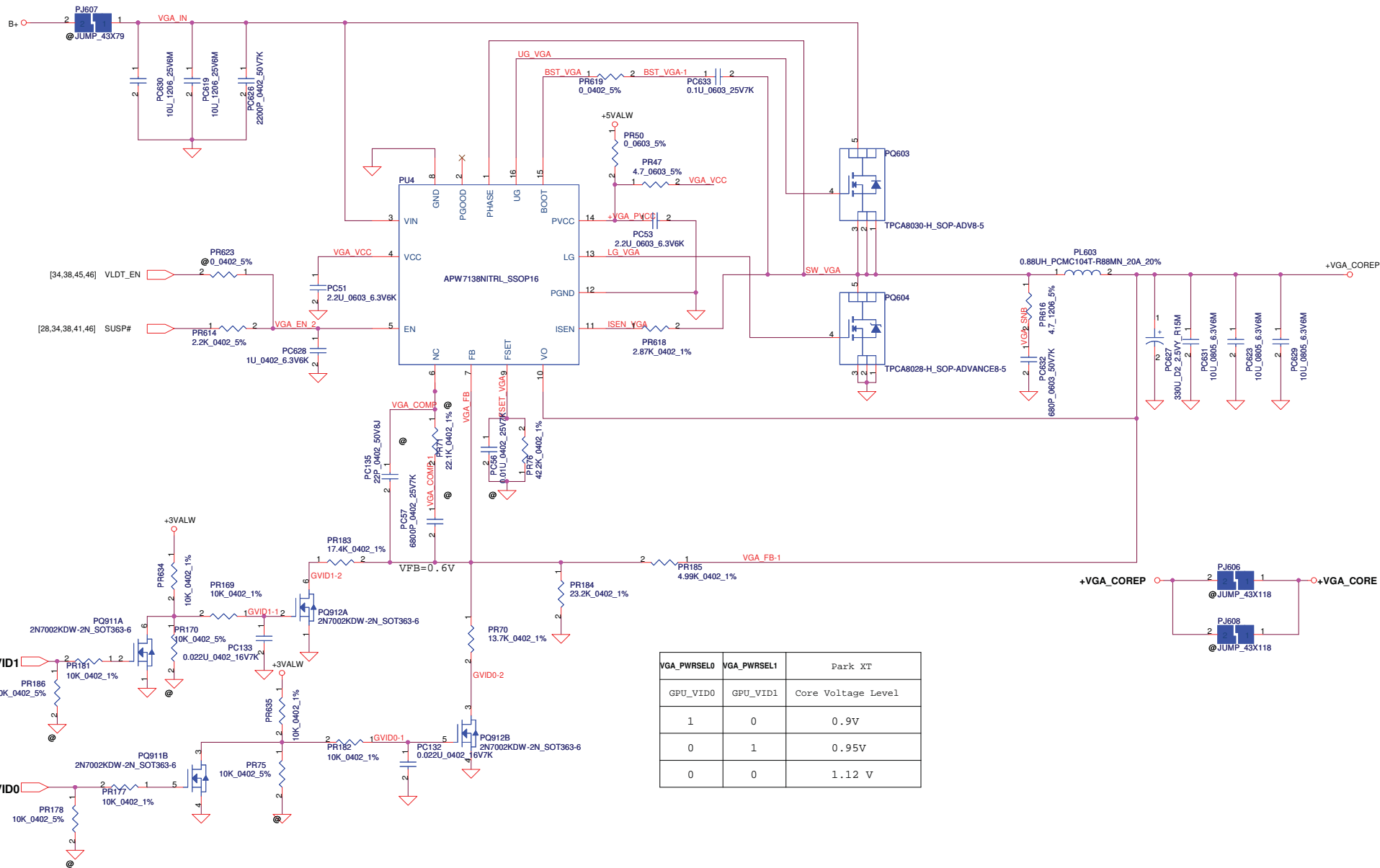
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title
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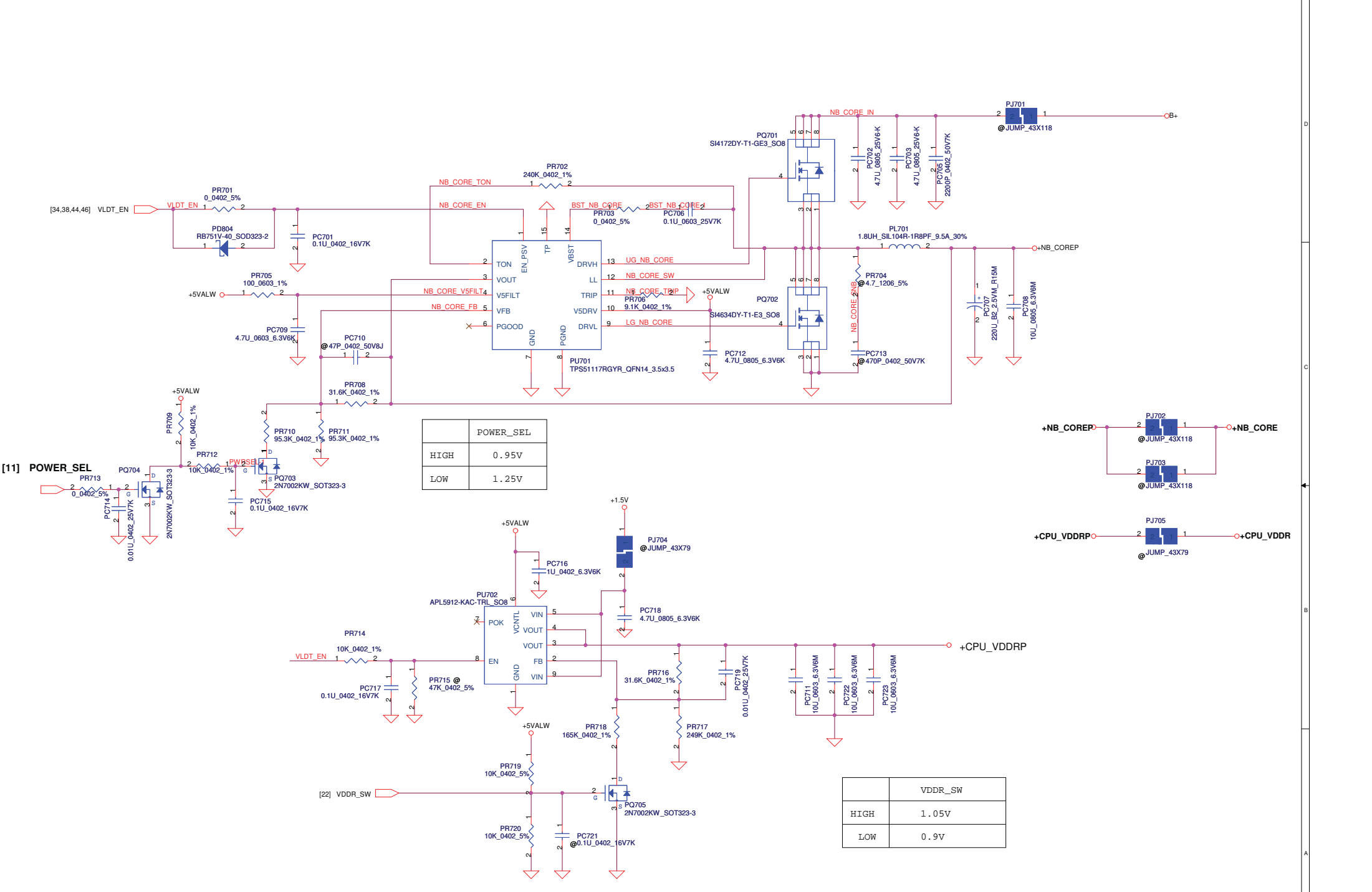


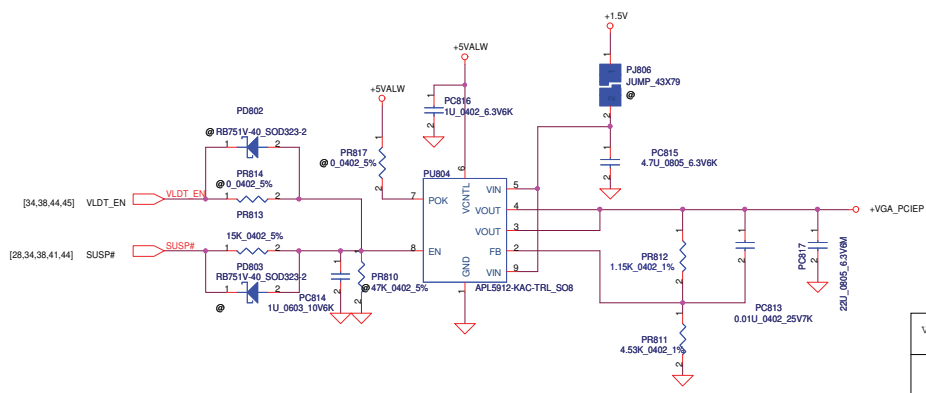
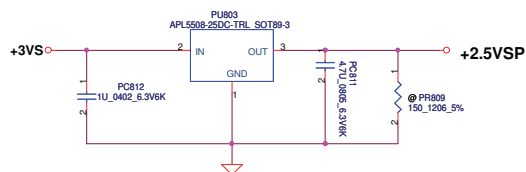


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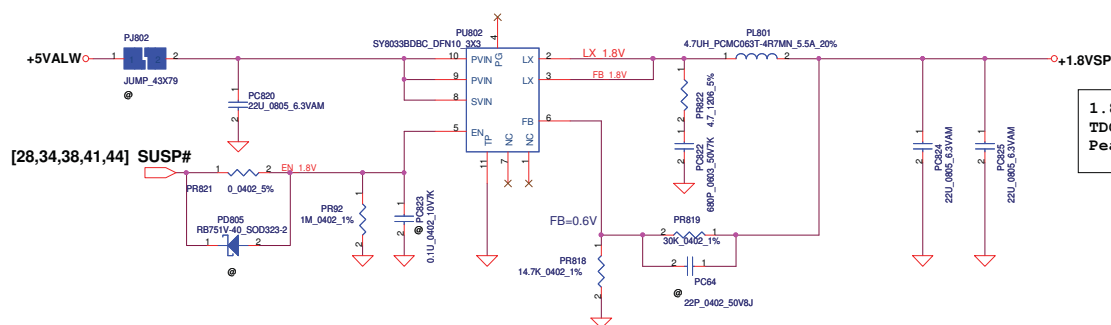
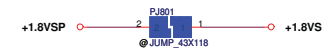
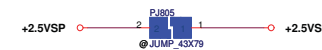


VGA_PWRSEL0	VGA_PWRSEL1	Park XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	0	0.9V
0	1	0.95V
0	0	1.12 V



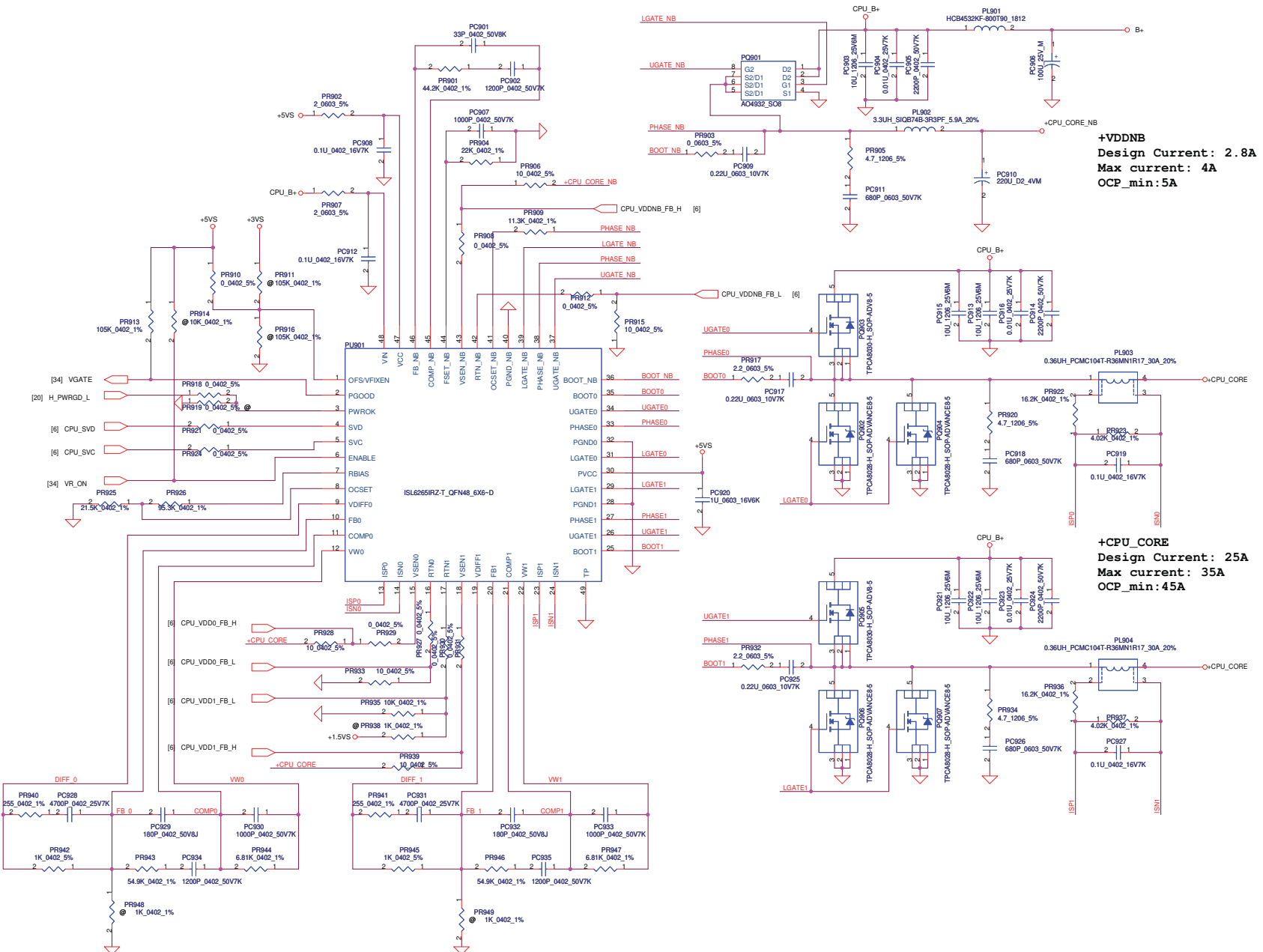


VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



1.8VSP  
TDC 2 A  
Peak Current 3 A

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**+VDDNB**  
Design Current: 2.8A  
Max current: 4A  
OCP\_min:5A

**+CPU\_CORE**  
Design Current: 25A  
Max current: 35A  
OCP\_min:45A